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REVIEW ARTICLE

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TWO STAGE CASCODE INDUCTIVE SOURCE DEGENERATION LOW NOISE AMPLIFIER IN 130NM 'RF CMOS'

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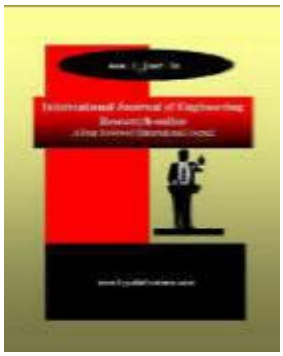


ABSTRACT

A two stage cascode CMOS Low Noise Amplifer(LNA) is implemented in 130nm RF CMOS technology with indcutive source degenration technique for low noise figure and power optimization using ADS tool for the frequency band of 2.4GHz with dc supply voltage of 1.3V. The 1st stage of LNA is designed basically for low noise figure and 2nd stage is designed for higher gain. The total dc current flowing through this circuit is 3.7mA.The designed LNA is biased with Active Bias technnique for better stablization and over temprature variation. The LNA acheives small signal gain of 30.1 db and 1.8dB noise figure. The input return and output return losses are -10.3 dB and -19.3 dB respectively. This circuit is designed for application in WiFi and Bluetooth.

Keywords :RFIC, Low Noise, RFCMOS, Cascode topology, inductive source degeneration.

INTRODUCTION

A Low Noise Amplifier (LNA) is the most critical block to determine sensitivity of a communication system [2]. Conventionalities GaAs and Bipolar technologies are used to implement the LNAs. Thanks the development of CMOS technology, it is possible to implement GHz RF and microwave circuits with sub-micron CMOS technologies. The CMOS technology has a merit to be combined with digital circuitries. Thus, CMOS LNAs have been extensively investigated in several papers. The cascode structure has been widely used for LNA designs because it is easy to satisfy both noise and power gain requirements [1].

CMOS technology is currently one of the dominant technologies used in the fabrication of consumer RF, analog, and digital integrated circuits mainly due to its low power consumption, low cost, and ease of integration. [2]

Design Approach

BLOCK DIAGRAM

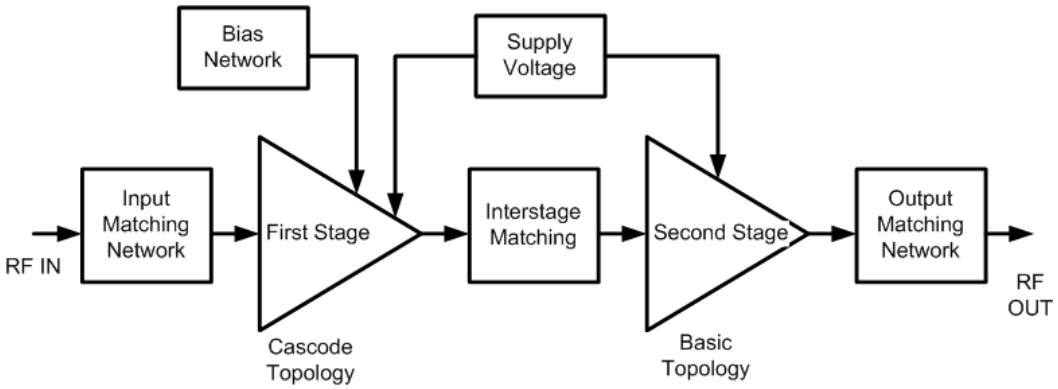
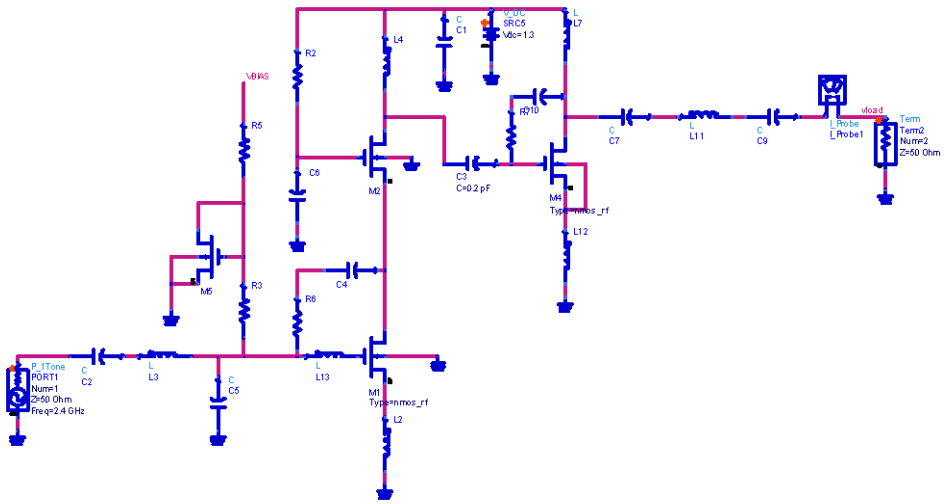


Figure 1: Block diagram of two stage CMOS Low Noise Amplifier

Above block diagram shows the complete structure of Low noise amplifier. As it is the two stage LNA, both stages connected with inter-stage matching and for it coupling capacitor is used. In designing an LNA, the following should be considered: power gain, noise figure (NF), impedance matching, reverse isolation, stability, distortion and power consumption. Input matching and Output matching networks are used for input and output stage respectively to minimize return losses which result in increased gain and output power. Input matching is done by calculation of input impedance using the ratio of the input voltage and input current. Passive elements having some impedance are connected at the input side, forming an input matching network to match this impedance. The loss occurred in this part of the circuit due to improper matching is known as Input return loss and denoted as S(1,1). The same concept is utilized to find S(2,2) at the output side.

COMPLETE TWO STAGE POWER AMPLIFIER

Figure 2: Schematic of complete Two Stage Low Noise Amplifier



First Stage

The first stage of typical CMOS low-noise amplifier uses an inductive degeneration approach for narrow-band input matching to the 50 Ω antennas. A cascode structure is also employed as it increases input-output isolation and output impedance for better stability and gain [2].

The transistor M1 is the main amplifying device of this stage and transistor M2 is cascaded with M1. To increase the gain and to minimize the current drawing capability here used cascode topology, this cascode topology called as current reused topology, it is called as current reused topology because whatever current consume by transistor M1 the same current will consume by M2. Basically the first stage is design for low noise figure and lowest power consumption

An inductor L4 of a large value is connected between the drain of M2 and Vdd. This inductor which opposes the change in current and the cascaded transistor is to prevent the large flow of drain current through M1 which can damage the transistor. The transistor M1 is biased with active current mirror bias technique through the resistor R3.As mentioned in the block diagram an input matching network is connected to the first stage i.e. the input stage for input impedance matching. The gate length of the transistors is fixed at 130nm and the width of gate is varied. The bulk of both the transistors is connected to ground. The output power of this topology is not as high as the power stage, but the isolation provided between output and input is very high. The dc current through this stage is 2.4 mA.

Second Stage

The second stage amplifier is a simple common-source architecture which is connected to the first stage through the coupling capacitor. The maximum current that this stage should consume is 1.3mA, thus a device size of 4um/0.13um was chosen. [2].Similar to first stage an inductor L7 of a large value is connected between the drain of the M4 and VDD, which is off-chip components, acting as RFC. This inductor opposes any change in dc current flowing through the drain and source of the transistor and thereby controls the flow of current through the transistor. The second stage is mainly design for higher gain.

Bias Network

As the first stage is the cascode structure of this LNA design biasing circuit is concern element & since it is an integrated circuit for biasing current mirror circuit has been used. So, transistor M1 biased with the help of the current mirror circuit. The bias circuits mainly design to drive main device of the circuit. For second stage biasing circuit is not used, at the gate terminal direct current is arrived from the first stage via coupling capacitor.

Input Matching

Impedance and noise matching are critical in LNA designs. In input matching, for simultaneous power and noise matching of multiple frequencies, the real part of Zin has matched to 50Ω and the imaginary part of Zin will be zero. For input matching filter is used for narrow band response at 2.4GHz. Input matching network is difficult to realize with CMOS so it is considered as off chip to reduce the chip size.

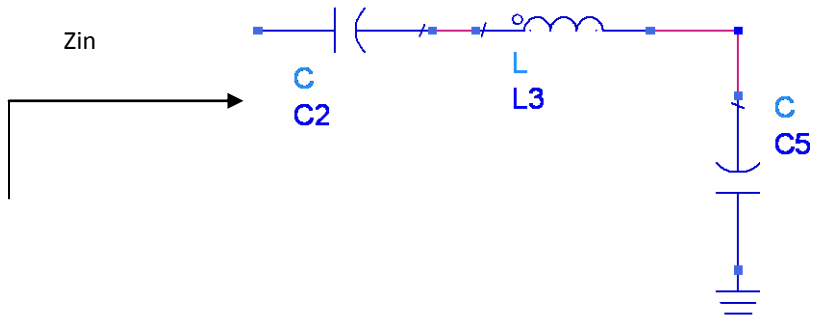


Figure 3: The input matching network

Output Matching

The output matching circuit is selected in that way, it improves the results and provide the best output return loss. At desired frequency bands, output return loss is -19.3 dB. It should exhibit high impedance at operational bands. That's not only reduced the chip size but also has a good output matching with much less chip area [4].

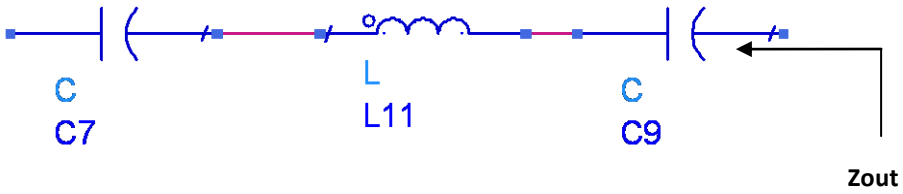


Figure 4: Output Matching Network

SIMULATION RESULTS

The LNA shown in Fig.1 was simulated by Advance Design System in TSMC 0.13 µm RF CMOS process. The layout of the LNA is shown in Fig.9. The chip area is 362 µm*200 µm including all bonding pads shown in fig11. The simulations, perform at schematic shows in fig2 gives good s-parameters performance. The two-stage cascode structure with inductive source degeneration LNA has good power gain and noise figure (1.8 dB) while consuming 0.4 mW of power, which are much better than the other comparative topologies. The complete circuit was simulated using ADS tool. Fig. 5, 6,7,8,9 and 10 show the LNA's simulated S21, S11, S22, S12, NF and stability of the LNA. At the center frequency f=2.4 GHz the gain the LNA is 30.1dB.

The input return loss [S11] is about -10dB, output return loss is about -19.3dB at 2.4GHz. The isolation is -61.7dB and the circuit is unconditionallyl stable.

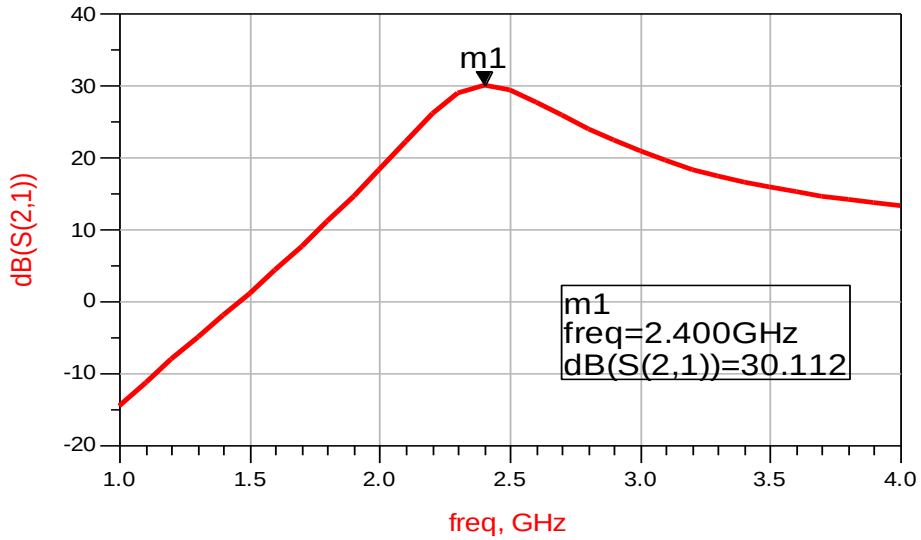


Figure 5: Gain

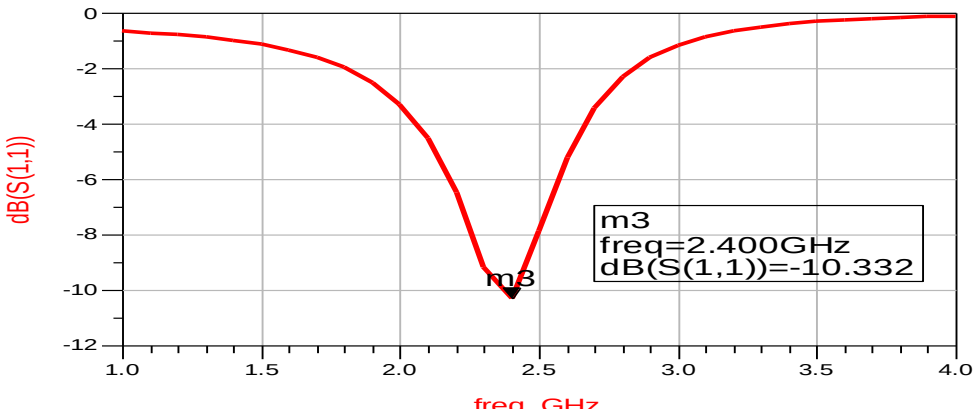


Figure 6: Input Return Loss

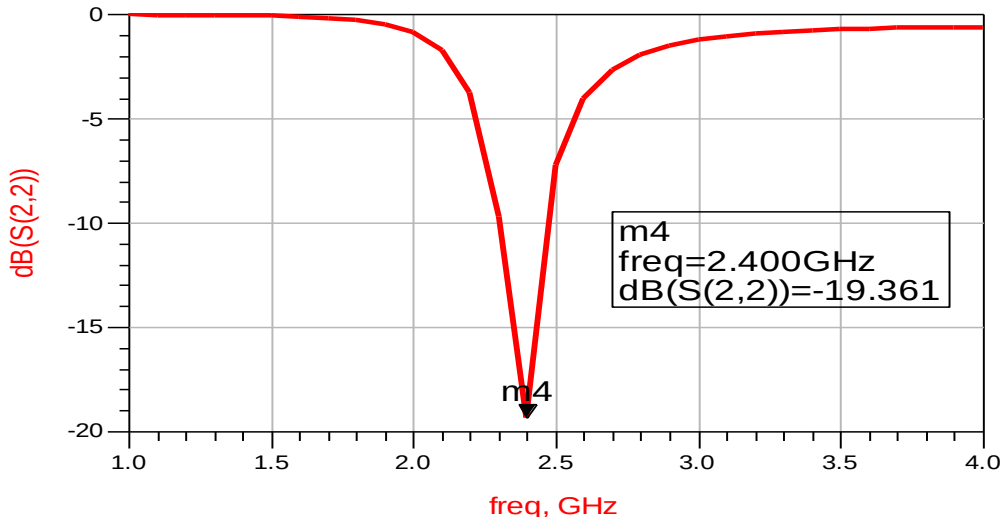


Figure 7: Output Return Loss

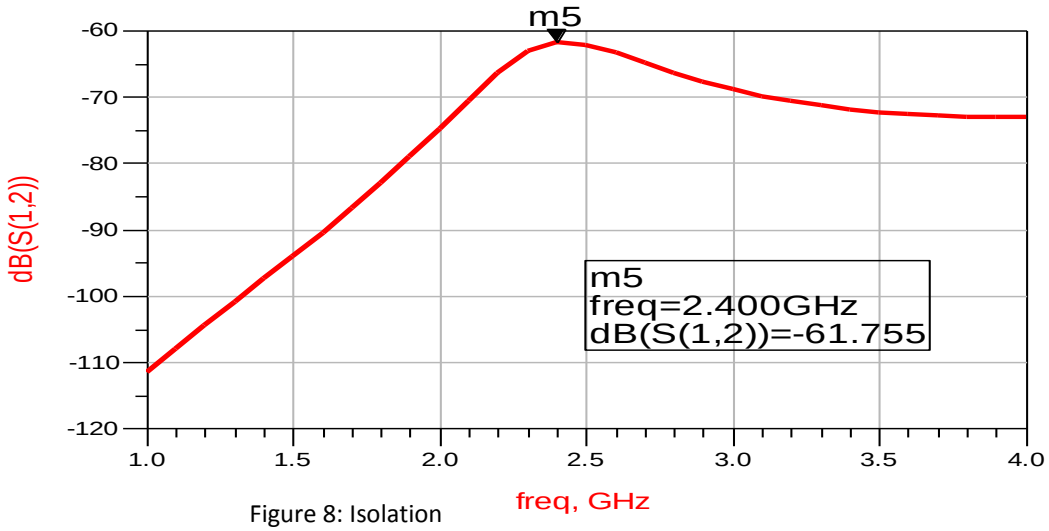


Figure 8: Isolation

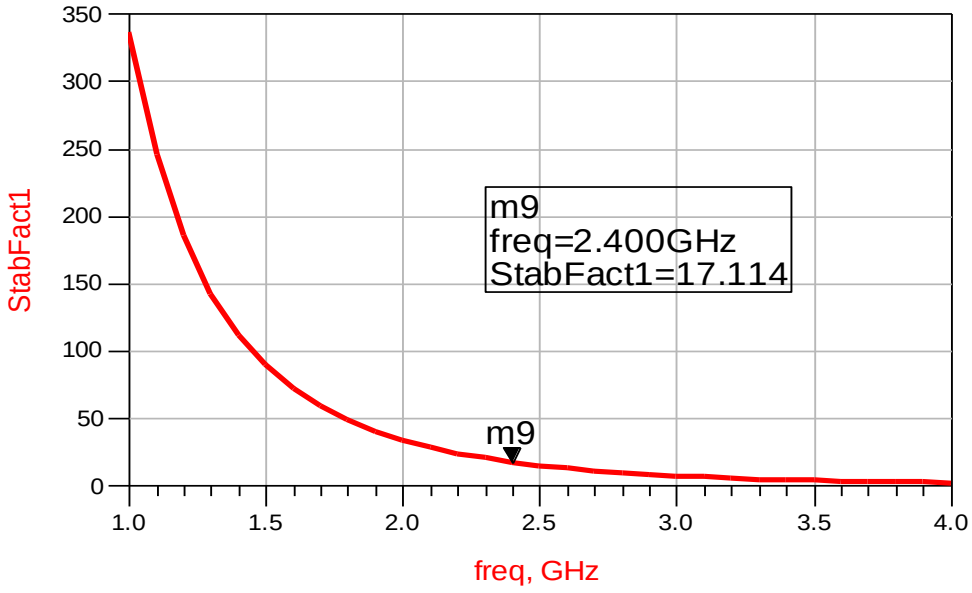


Figure 9: Stability

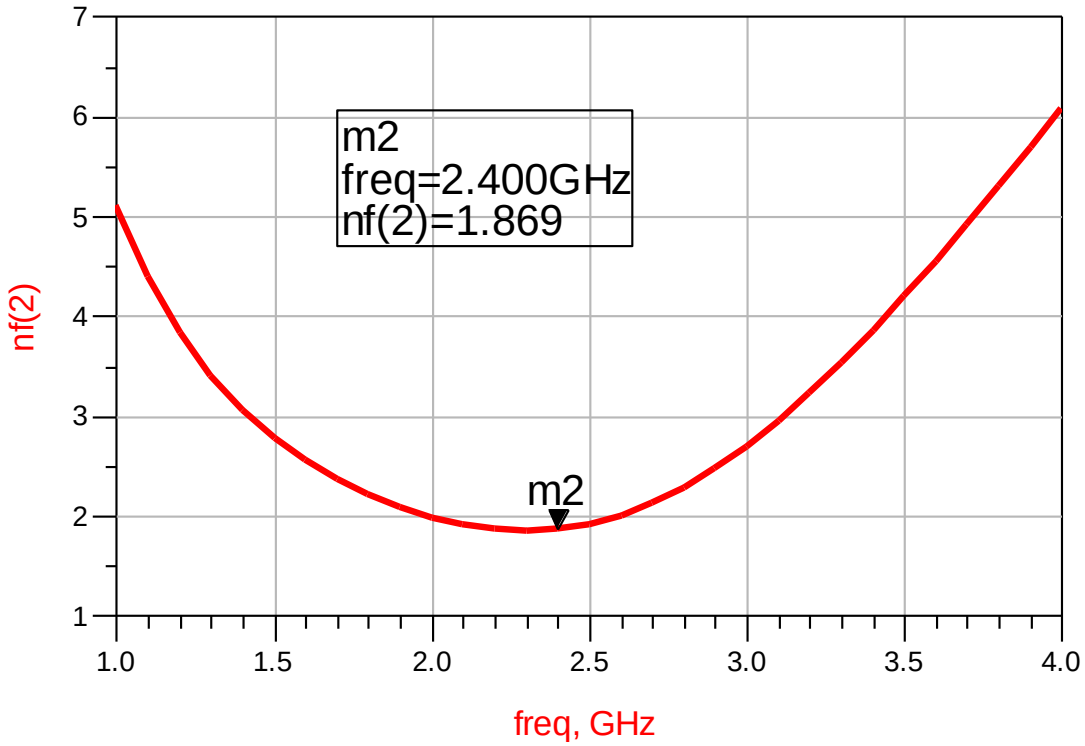


Figure 10: Noise Figure

Table1: CMOS Low Noise Amplifier Specification

Parameters	**Value**
Operating Voltage	1.3V
Technology	0.13 µm RF CMOS process
Operating Frequency	2.4 GHz
S (2,1) Gain	30.1dB
S (1,1) Input Return Loss	-10.3dB
S (2,2) Output Return Loss	-19.3dB
S (1,2) Isolation	-61.7dB
NF	1.8dB
Total Power Consumption	4.8mW
Total DC Current	3.7mA

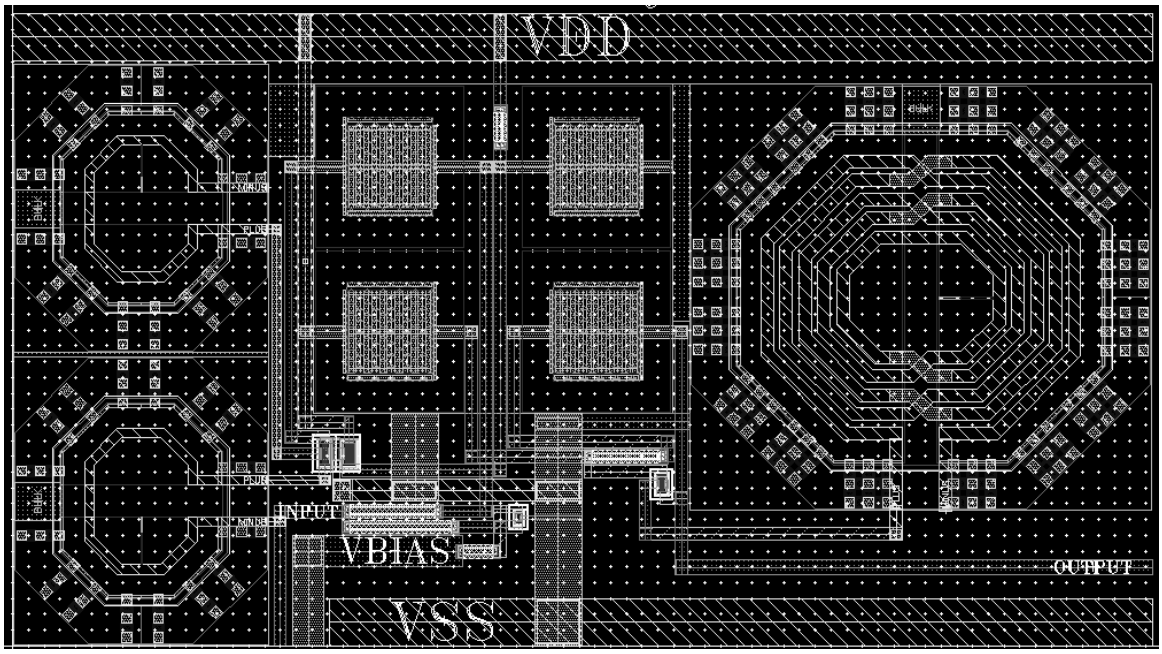


Figure 11: Layout

CONCLUSION

An approach for designing low-voltage, low-power inductively degenerated CS LNAs is presented for the wireless applications. The tool used for designing this circuit are ADS (Advanced Design System) tool of Agilent Systems. This circuit designed in RFCMOS 0.13µm technology provided by ADS tool. Simulation results show that gain, low noise, good isolation and stability are simultaneously achieved by a low noise amplifier. The result of the LNA is summarized in the table 1.

The Interstage coupling capacitor is used to achieve the high gain. The gain is about 30.1dB has been achieved in all the frequency bands of interest with 1.8 dB noise figure.

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