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A SURVEY ON SOFT ERROR ESTIMATION FOR SRAM BASED FPGAS

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ABSTRACT

Radiation-induced soft errors are an increasingly important threat to the reliability of integrated circuits (ICs) fabricated in advanced CMOS technologies. Soft errors are events in which data is corrupted, but the device itself is not permanently damaged. In contrast, a permanent device failure is called a hard error. Soft errors can have different effects on applications. On the one hand, they may result in data corruption at the system level, which may or may not be detected.FPGAs provide an attractive design platform because of their short design cycle and low development cost. With exponential growth in performance and capacity, SRAM-based FPGAs are widely used in many application domains such as telecommunication, industrial control, and embedded applications. Even in the aerospace domain, aircraft designers try to apply SRAM based FPGAs in electronic systems because they offer a significant advantage in high density and on-orbit programmability.As the feature size shrinks to the nanometer scale,SRAM-based FPGAs will become increasingly vulnerable to soft errors. In this paper let us have a brief survey on soft errors and soft error estimation methods for SRAM based FPGAs including soft error overview, FPGA failure models, Need of soft error estimation.

Keywords – SRAM based FPGAs,soft error,failure models,Failure in Time,test cube,trace, Soft error rate,Error propagation probability.

INTRODUCTION

SRAM based FPGAs became a universal and cost effective platform for a lot of applications including prototyping, small productions and application requiring during lifetime or dynamic reconfiguration. But one of the challenges followed by FPGAs is its vulnerability of configuration memory to "soft errors".According to NASA Thesaurus [5] radiation induced soft errors in microelectronic circuits caused when chargedparticles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass

leaving behind a wake of electron hole pairs. As the technology of FPGA device evolve rapidly as well as the size of the bit errors in the configuration memory are becoming a significant in vulnerability issue of modern FPGAs.An FPGA as a universal device does not typically require all the programmable resources of FPGA to be active.On the contrary majority of configuration memory is not used and a single error in the unused part has no effect.The classification of those bits requires a precise knowledge of the FPGA basic structure as well as the exact assignment of configuration bits to the FPGA resources.For simple circuits the number of sensitive bits will also be smaller.The main challenge of soft errors is the continuous downscaling of technologies which results the clock frequencies reaching multiples of GHz range, supply voltage decreasing below one volt level and load capacitances of circuit needs dropping to femto farads.

Soft errors are caused by an radiation induced energetic particle like neutrons,alpha particles coming from the cosmic rays and chip packaging[4].These particles can generate a dense track of electron hole pairs as they pass through a semiconductor device.This phenomenon is referred to as Single Event Transient (SET) [4].Due to their high charge collection efficiency the reverse biased pn junctions in an IC are the most susceptible parts of SETs.If a sufficient amount of charge is collected by the junction, the SET results in a fault by flipping the logic state ("1" to "0" or vice versa).When such faults are latched into a memory cell soft errors will occur. Although soft errors do not damage the device it poses a potential threat to the reliability of the circuit. If uncorrected, soft error causes a failure rate higher than the rate of all hard failure mechanisms. Typically hard failure rates add up to 50 to 200 FIT (Failure in Time: 1 fail per 10^9 device operation).In fact soft errors have been always a key reliability concern for SRAM based FPGAs using for mission critical applications where a single error can cause can lead to catastrophic errors. Examples include space borne electronics, aircraft controllers, military electronics etc.

SOFT ERROR OVERVIEW

The soft error at ground level was first reported by May and Woods in DRAM in 1978 [7].The impact of soft error is not severe at ground level. A soft or non-permanent fault is a non-destructive fault and falls into two categories namely transient fault and intermittent faults. Transient faults caused by environmental conditions like temperature, humidity, pressure, voltage etc. Intermittent faults caused by non-environmental conditions like loose connections, aging of components, critical timing etc. Soft errors are a subset of Single Event Effects[14] and can be classified as follows:

- Single Bit Upset: A particle strike causes a bit flip in a memory cell.
- Multiple Bit Upset:The event causes the upset of two or more bits in the same word.
- Multiple Cell Upset: The event causes the upset of two or more memory or latches.
- Single Event transient: The event causes a voltage glitch in a circuit which becomes a bit error when captured in a storage element.

Soft error sources

Three particle sources have been identified namely alpha particles, neutrons, and the secondary radiation produced from the interaction of cosmic ray neutrons and boron.

(a) Alpha particle: Alpha particles are the nuclei of helium atoms. They interact strongly with the matter and heavily ionizing. Typical alpha particle energy is 5MeV with a typical range of 50mm in air and 23μ in silicon.

(b) Neutrons: High energy neutrons from cosmic radiation can induce soft errors in semiconductor devices via secondary ions produced by the neutrons. Neutrons are more likely cosmic radiation sources to cause SEU in deep submicron semiconductors.

(c) Secondary radiation produced from the interaction of cosmic ray neutrons and boron.

The secondary radiation is induced by low energy cosmic neutrons interacting with the isotopes of boron. Boron is widely using as the p-type dopant in silicon. Thereaction mechanism is shown in the Fig 1.

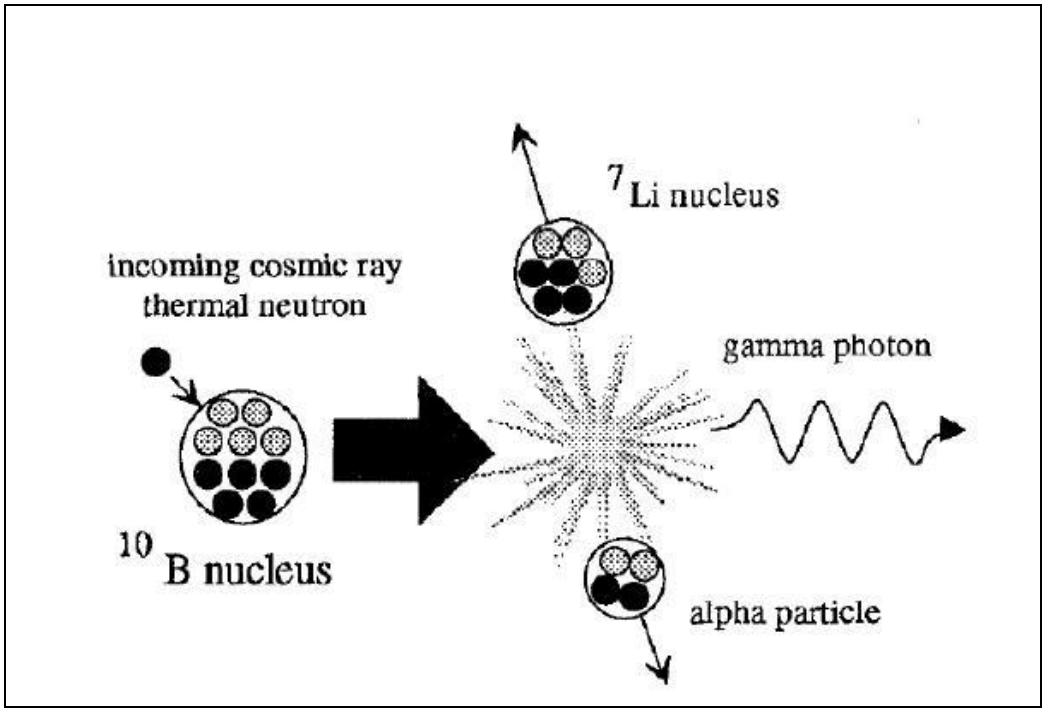

Fig 1 Secondary radiation produced as a result of interaction of cosmic rays and boron.

SOFT ERRORS IN SRAM BASED FPGAs

FPGAs (Field Programmable Gate Array) are the most flexible logic device that contains a matrix of reconfigurable array logic circuitry. The configuration of an FPGA has a form of a file. It contains the configuration state of all resources include Look Up Table, switch matrix etc. [15]. The FPGA architecture is mainly defined by its switchmatrix. The programmable switchbox contains wires and switches that connect wire segments.The active set of those switches form the desired connections of the switch box.

FPGA Configuration

The configuration of FPGAs is normally stored in either SRAM (Static Random Access Memory), aflash, or EEPROM cell. In SRAM based FPGAs can indefinitely reconfigure. They therefore have simple development mechanics. They can also be changed by reconfiguring with new code, a feature attractive to designers. The content of the FPGA configuration SRAM is typically routed bit by bit directly to the FPGA devices where it controls its function and routing. Thebit stream of configuration memory is depends on the circuit description in a high level description language and the set of constraints and the tools provided by the FPGA manufacturer(Xilinx) or a third party such as Cadence.

Soft error failure models in SRAM based FPGAs

FPGAs have many Single Event Upset induced failure modes, for example even by changing any one of the configuration bit, a Look Up Table (LUT) function will gets diverted. There are many ways to classify the soft error failure modes of FPGAs.Widely the classification is based on the routing errors and logic errors. Seven failure modes are considered here which are listed below.

(a)Mux selectfailure.

Multiplexers are a part of routing network, very sensitive to single event upset because a change in their select lines will cause a different routing configuration.

(b)Programmable Interconnect Point failure.

A Programmable Interconnect Point (PIP) is a pass transistor between two wires that can either be on or off.PIP failure is of PIP short and PIP open. A PIP failure causes the interruption of data flow.

(c)LUT Upset

LUT value change comes under the logic value change. This failure mode will change the function of the implemented design.

(d)Buffer failure modes

In an FPGA buffer act as a driver which can either are turned on or off. A buffer has two failure modes namely buffer short and buffer open.

NEED OF SOFT ERROR ESTIMATION

Radiation induced soft error have become one of the most important and challenging failure mechanism in modern electronic devices especially in modern electronic device like FPGAs.SER (Soft Error Rate) for commercial chip is controlled to within 100-1000 FIT.The story of SER problem in the Intel 2017 series is well discussed in the IBM journal of Research and Development of January 1996 [8].IBM measurements provided evidence that at sea level cosmic radiation contributes SER and its effects increases exponentially with altitude[12,13].In 1975 Binder published the first report of soft errors in space applications[17].At the time when SER was discovered as an important reliability issue for space applications,SRAM were most robust to soft errors. This is mainly caused by downscaling of the supply voltage and by the reduction of feature sizes. Cohen published one of the SER trends in [18].They determined experimentally that as the feature size decreases the soft error rate increases, demonstrated in Fig 2.

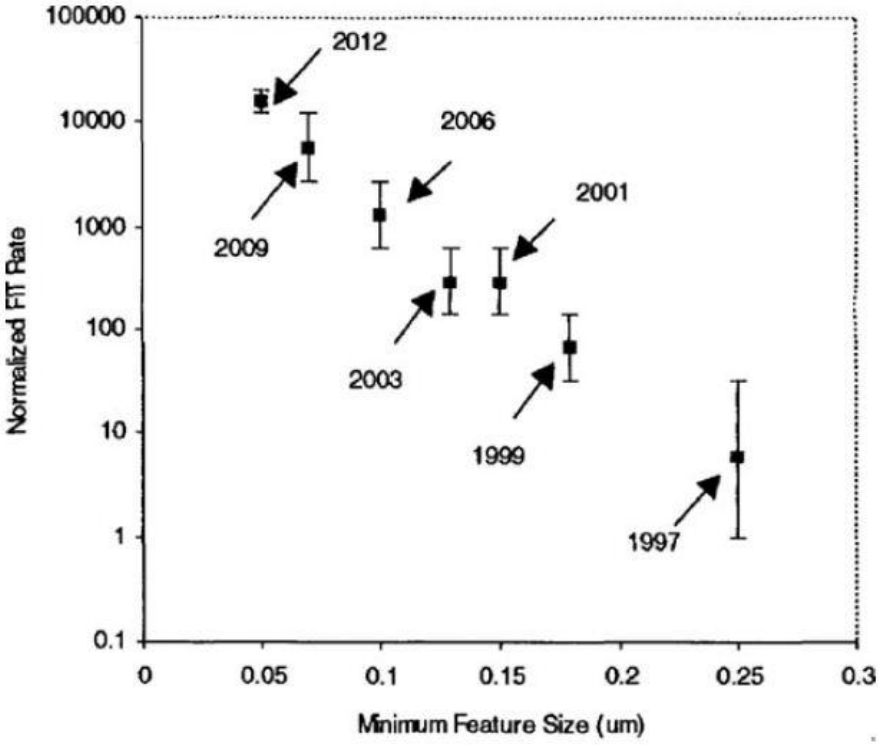

Fig 2 Scaling trend of FIT/Mbit of SRAM(figure from [18]).

SOFT ERROR ESTIMATION METHODS

A.SER Estimation based on propagation probability.

The soft error rate can be estimate by static analysis in which error propagation rules are used for the estimation of error rate.It involves three steps namely path construction,Ordering [21] and Error Propagation Probability(EPP) computation.The first step involves selecting the paths which are affected by error using Depth First Search algorithm [18].Next levelize signals on topological order. Last step will find out the EPP by using propagation rules.

B. Simulation based analysis of SEU effects in SRAM based FPGAs

Simulation based analysis [22] of FPGAs combines radiation testing with simulation. The radiation testing is used to set on technology on which the FPGA device lies; it doesn't matter about what kind of circuit it implements. The second element that is simulation is used to predict the probability of an SEU which change the expected response of the circuit mapped on the FPGA. Thus by combining these two elements compute the device cross section of the circuit mapped on the FPGA.Several simulation tools are using for the fault injection and analysis. These tools will identify the FPGA resources that are used and then it generates the fault list to be injected. During simulation the outputs produced

by the faulty will be comparing with the fault free. To estimate the accuracy of the tool compare the output response with the actual response.When a mismatch occurs on the output values the test will stops.

C. Reliability evaluation of SRAM based FPGA design

FPGAs are widely susceptible to soft errors, so the reliability evaluation in terms of soft error is essential. A mathematical model called "series model" [23] is used as the reliability model. Here considers the FPGA is in running on a non-redundantfailure, and all failures considered being statistically independent. Thus the overall failure will be the sum of all failure rates. For SRAM based FPGAs the overall reliability will be the product of two terms one represents the reliability of the device with respect to functional failure and other representing the reliability of the device based on the physical failures. The reliability of the can be calculated as the number of failures observed in a group of devices during a unit time event.

D. Improving Soft error tolerance of FPGA

In this approach Asymmetric SRAM (ASRAM) structure proposed to optimize immunity against soft errors. To reduce SER estimation "bit inversion"technique [24] is proposed. This technique will reduce the number of ones stored in a LUT.LUT is rearranged to if it contains more number of zeros than ones to maintain the correct functionality of the FPGA. The use of ASRAM for the configuration memory may results in the reduction of leakage power when the ASRAM cell in its preferred state.

E.Device and Architecture concurrent optimization for FPGA transient Soft error rate.

Here an efficient and accurate SER estimation method called "trace" method is proposed for error estimation.For error estimation at first collect the statistical information called trace information [25]. Two types of trace information are used. The first type is logic probability and the second one is the average logic sensitivity. Here the logic sensitivity is calculated for each input of gate. For each input vector first traverse the circuit and then evaluate the logic value and logic sensitivity for each gate input and output. Then calculates the logic probability for each gate by applying input vectors.

PROPOSED METHOD FOR SOFT ERROR ANALYSIS

The reliable method for soft error estimation is based on "test cube based method". For error estimation here we need only aware about cubes and covers for particular output. Cube[26]defines the relationship between input and outputs. A cover is defined as the set of cubes that gives same output. Two pass method is using for estimating Error Propagation Probability of SRAM based FPGAs.In the first pass ,forward pass logic simulation will be performed. In the second pass, backward pass computes the care cover. The care cover is defined as the set of cubes which will propagates the faulty logic value. For the combinational logic mapped on FPGA EPP of a fault will be the ratio of the vectors represented in the care covers to the total number of input vectors.

FUTURE TRENDS

About one decade ago ,the Soft Error Rate(SER) is growing due to increase in Failure In Time (FIT) peer bits of SRAM based FPGAs.With technology scaling the FIT per bits of SRAM based FPGA are the most vulnerable parts in the process technologies.SER of a system is an important reliability risk or not strongly depends on its application. For applications such as car radio, mobile phones SER levels are acceptable than for a critical applications. So application mission profile of the system plays an important role in risk assessment.One of the important problems is the contribution of alpha and neutrons in soft errors.In early 1980s most of the SER related problems was induced by alpha particles. Moreover a typical concentration of radioactive impurities has been reduced for the FPGAs for which soft error rate is more. With technology scaling results in a lower critical charges, thecontributions of alpha particles in soft error is unavoidable factor.

In the last 25 years many investigations have been spent to study soft error subject. This trend will continue in coming years because SER become a reliability risk for more and more applications. In the future it will be increasingly important to have assessed the solution for SER estimation, since there will be more number of SRAM cells per FPGAs.Also in future, wear out mechanism may cause an increase in threshold voltages of the transistors. Therefore the critical charges decreases and the circuits become more susceptible to soft errors.

CONCLUSION

Due to the continuous device scaling SRAM based FPGAs will become more vulnerable to soft errors by changing the FPGAs configuration memory may affect dramatically the functions implemented by the device.So soft error estimation is very essential for FPGAs. Recent researches put forward some techniques for soft error estimation based on error propagation probability and node error rate. The soft error rate per bit of the most vulnerable components (SRAM, sequential logic) can be decreased in more advanced process technologies. Because of increasing system sizes and complexities upcoming investigations will be necessary to curtail the reliability risk for FPGA devices

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