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RESEARCH ARTICLE

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AN EFFICIENT ANT ARCHITECTURE FOR RELIABLE LOW POWER MULTIPLIER DESIGN WITH FIXED-WIDTH RPR

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ABSTRACT

In this paper we proposed a reliable low power multiplier design for fixed-width RPR to resolves the following parameters. In order to meet the demand of high accuracy, minimum power consumption, and good area efficiency we also include the use of ANT architecture. We design the fixed–width RPR with error compensation circuit. The hardware complexity of the error compensation circuit will be low.

Key words—Algorithmic noise tolerant (ANT), Reduced-precision replica (RPR).

I. INTRODUCTION

The rapid growth of portable and wireless computing systems in recent years drives the need for ultralow power systems. To lower the power dissipation, supply voltage scaling is widely used as an effective low-power technique since the power consumption in CMOS circuits is proportional to the square of supply voltage [1]. A novel algorithmic noise tolerant (ANT) technique [2] combined VOS main block with reduced-precision replica (RPR), which combats soft errors effectively while achieving significant energy saving. Some ANT deformation designs are presented in [12]–[9] and the ANT design concept is further extended to system level in [10]. However, the RPR designs in the ANT designs of [12]–[7] are designed in a customized manner, which are not easily adopted and repeated. The RPR designs in the ANT designs of [6] and [9] can operate in a very fast manner, but their hardware complexity is too complex. As a result, the RPR design in the ANT design of [2] is still the most popular design because of its simplicity. However, adopting with RPR in [2] should still pay extra area overhead and power consumption. In this paper, we further proposed an easy way using the fixed-width RPR. In order not to increase the critical path delay, we restrict the compensation circuit in RPR must not be located in the critical path. As a result, we can realize the ANT design with smaller circuit area, lower power consumption, and lower critical supply voltage.

II. ANT Architecture Designs

The ANT technique [2] includes both main digital signal processor (MDSP)

and error correction (EC) block. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay T_{cp} of the system becomes greater than the sampling period T_{samp}, the soft errors will occur. It leads to severe degradation in signal precision. In the ANT technique [2], a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block. Under VOS, there are a number of input-dependent soft errors in its output $y_a[n]$; however, RPR output $y_r[n]$ is still correct since the critical path delay of the replica is smaller than T_{samp} [4]. Therefore, $y_r[n]$ is applied to detect errors in the MDSP output $y_a[n]$. Error detection is accomplished by comparing the difference $|y_a[n] - y_r[n]|$ against a threshold Th. Once the difference between $y_a[n]$ and $y_r[n]$ is larger than Th, the output $\hat{y}[n]$ is $y_r[n]$ instead of $y_a[n]$. As a result, $\hat{y}[n]$ can be expressed as

$$\hat{Y}[n] = \begin{cases} Y_a[n], & \text{if } |Y_a[n] - Y_r[n]| \le Th \\ Yr[n], & \text{if } |Y_a[n] - Y_r[n]| > Th \end{cases} \quad (1)$$

Th is determined by

$$Th = \max |Y_o[n] - Y_r[n]| \quad (2)$$

Where $y_o[n]$ is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation [2]. And comparing with the Full-Width RPR the Fixed-Width RPR has great advantage. That the power, area, and time (delay) are also comparably reduced.

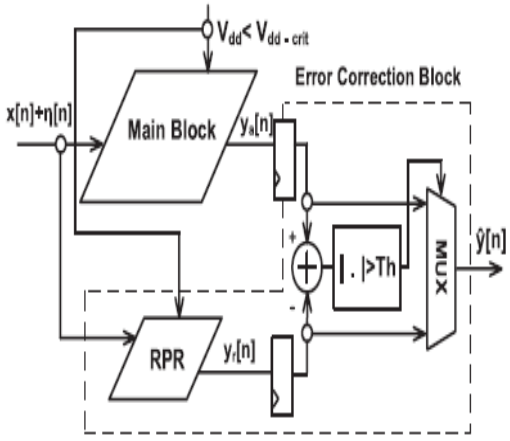

Fig. 1 ANT Architecture design

III. ANT ARCHITECTURE WITH FIXED-WIDTH RPR

In this paper, we further proposed the fixed-width RPR block in the ANT design [2], as shown in Fig. 2, which can not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating supply voltage, and lower power consumption in realizing the ANT architecture. We demonstrate our fixed-width RPR-based ANT design in an ANT multiplier. The fixed-width designs are usually applied in DSP applications to avoid infinite growth of bit width. Cutting off n-bit least significant bit (LSB) output is a popular solution to construct a fixed-width DSP with n-bit input and n-bit output. The hardware complexity and power consumption of a fixed-width DSP is usually about half of the full-length one. However, truncation of LSB part results in rounding error, which needs to be compensated precisely. Many literatures [13] have been presented to reduce the truncation error with constant correction value [13] or with variable correction value [5]. The circuit complexity to compensate with constant corrected value can be simpler than that of variable correction value; however, the variable correction approaches are usually more precise.

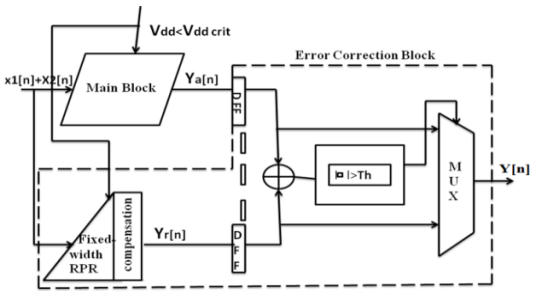

Fig.2 proposed ANT architecture with Fixed-width RPR

IV. MAIN BLOCK

The main block which consisting of multiplier. In the existing ANT multiplier design consist of the Baugh-Wooly multiplier. It has the normal design of half adders and full adders. Baugh-Woolley Multiplier is a high speed multiplier using the shift and adds method. This parallel multiplier uses lesser adders and minimum iterative steps. As a result of which they occupy minimum space as compared to the serial multiplier. It is very special criteria because in the fabrication of chips and high performance system requires components which are as small as possible. Experimental

result demonstrate that the proposed circuit not only improves the accurate performance but also reduces the hardware complexity and also less power consumption that is dynamic power of 15.3mW and maximum clock period of 3.912ns. But in the proposed multiplier design is uses the Wallace tree multiplier. That is also having its own regular structure. It even reduces the amount of full adders and half adders used. Wallace tree multiplier consists of three step process, in the first step, the bit product terms are formed after the multiplication of the bits of multiplicands and multipliers, in second step, the bit product matrix is minimized to lower number of rows using half and full adders, this process will follows till the last addition remains, in the final step, finally addition is done using adders to obtain the result [8]. Here we are using the 4×4 structure design.

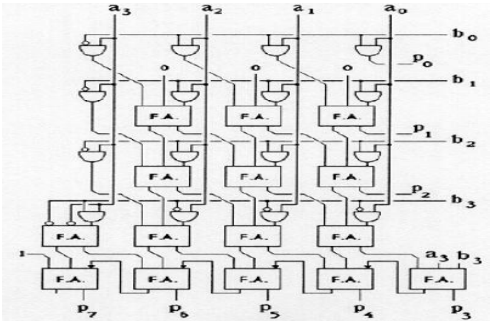

Fig.3 4×4 Baugh-Woolley Multiplier

V. ERROR CORRECTION BLOCK

That the error corrections block which consist of multiplexer, RPR block compensation circuits and flipflop.

A. Compensation Circuit And Flipflop

The error compensation circuit which is combined with the RPR block. And the error which is not placed in the critical path. So, the error compensation will be easier one. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay T_{cp} of the system becomes greater than the sampling period T_{samp}, the soft errors will occur. It leads to severe degradation in signal precision. In the ANT technique [2], a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block. In many high-speed digital signal processing (DSP) and multimedia applications, the multiplier plays a very important role because it dominates the chip power consumption and operation speed. In DSP applications, in order to avoid infinite growth of multiplication bit width, we usually have to reduce the number of multiplication products. Cutting off n-bit less significant bit (LSB) output can construct a fixed-width multiplier with n-bit input and n-bit output. However, truncating the LSB part leads to a large number of truncation errors. Many truncation error compensation techniques have been presented to design an error compensation circuit with less truncation error and less hardware overhead. The compensation methods can be divided into two categories: compensation with constant correction value and compensation with variable correction value. Circuit complexity to compensate with constant corrected value can be simpler than that of variable correction value; however, the variable correction approaches usually can be more precise [4].

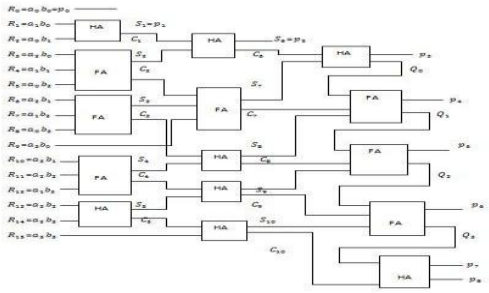

Fig.4 4×4 Wallace tree Multiplier

Both the outputs [$Y_a[n]$ and Yr[n]] of main block and the RPR block output are sent by using two D Flip flops. Normally we may use the registers also. But comparing with the flipflop the registers are accuracy wise low, so it better to use flipflop. Here we use the D flipflop as the delay flipflop. Because that the one bit delay period is used to compare the two outputs $Y_a[n]$ and Yr[n].

B. Multiplexer

In order to get the output from the flip flops we have a two 21 multiplexer. The two inputs are from the main block $Y_a[n]$ and the RPR block Yr[n]. The selection line which is used to the formula in equation (2).

VI. PERFORMANCE COMPARISON

That the following comparison table shows the details between the designs of Fixed-Width RPR and Full-Width RPR. In those table three parameters has explained.

TABLE I: Comparison between Fixed-Width RPR and Full-Width RPR

Parameter	Full-Width RPR	Fixed-Width RPR
Delay(ns)	50.59	41.48
Area(Gate count)	4,809	4,671
Power(µw)	63	58

And the next coming table 2 will shows the comparison between two RPR designs, but the Fixed-Width RPR uses the Wallace tree Multiplier instead of using Baugh-Woolly Multiplier. And this will be designed by using TANNER software.

TABLE II: Comparisons between Baugh-Woolly Multiplier and Wallace Tree Multiplier

Parameter	Baugh-Woolly Multiplier	Wallace Multiplier
Delay(sec)	121.25	71.26
Area(Gate Count)	3846	3812
Power(µw)	$8.627835e^{-4}$	$1.270499e^{-2}$

VII. SIMULATED RESULTS

The Multiplier is simulated by using MODELSIM software is shown in Figure 4. Here the two inputs are X and Y.

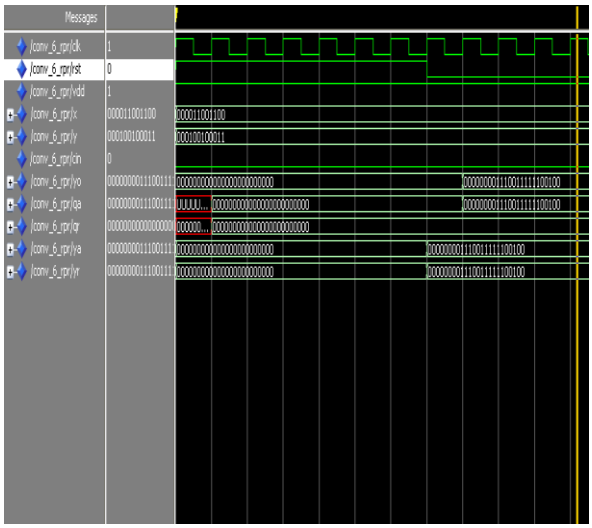

Fig.5 Simulation output of ANT Multiplier with Fixed-Width RPR

The Multiplier is simulated by using TANNER software is shown in Figure 5. Here the two inputs are X and Y.

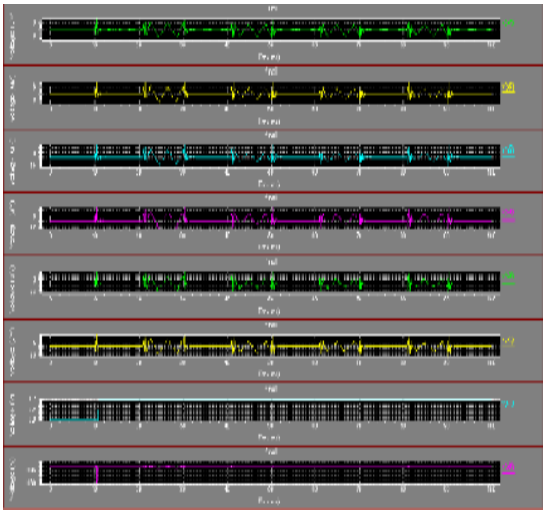

Fig.6 Simulation output of ANT Multiplier with Fixed-Width RPR using Wallace Multiplier

VIII. CONCLUSION

Full-width RPR-based ANT multiplier design has a lot of disadvantages. So the proposed Fixed-width RPR based ANT architecture with baugh-wooly multiplier circuit has overcomes the demerits. It has *1V* supply voltage and 24.103-MHz operating frequency, the power consumption is 0.393 µw. Area of this fixed-width RPR can be saved by 45% and power consumption can be saved by 18%. And by using Fixed-width RPR based ANT architecture with Wallace tree multiplier circuit even reduce the amount of power and time.

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