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VERSATILE MODIFIED BOOTH RECODER USING SQRT CSLA BASED S-MB RECODING TECHNIQUE

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ABSTRACT

The Modified Booth Recoding method is widely used to generate the partial products for implementation of large parallel multipliers which adopts the parallel encoding scheme. In this work an optimizing the design of the Fused Add Multiply (FAM) operator for increasing the performance. Modified Booth form is used to implement the direct recoding of sum of two numbers. The efficient recoding technique that implement in three different schemes in single precision FAM unit. In the FAM design Square Root Carry Select adder (SQRT) is used to reducing the half of the area compared to the previous methods. To eliminate the truncation error in the design by using Multi Level Conditional Probability (MLCP) estimator. MLCP estimator using the non zero code to estimate and avoid the truncation error and achieving high accuracy.

KEYWORDS:SQRT CSLA adder, MLCP Estimator, S-MB recoding

I.INTRODUCTION

The Multiplier and the Multiply and Accumulator(MAC) are the essential elements of the digital signal processing such as filtering, convolution. The speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire calculation. Because the multiplier requires the longest delay among the basic operational blocks in the digital system. For high speed multiplication, the modified radix-4 Booth algorithm is commonly used. The modified booth recoding technique that reduce the number of partial products. the three steps of the multiplications are, 1) Partial Product Generation (PPG), 2) Partial Product Reduction (PPR), 3)Carry Propagate Addition (CPA) based on this steps the modified booth multiplier process for the high speed functions.

The first is booth recoding in which a partial products is generated from the multiplicand and multiplier. The second is adder array or partial product compression to add all partial products and convert them into the form of sum and carry. The last is the final addition in which the final

multiplication result is produced by adding the sum and carry. In this sum modified technique propose that compress the add and multiplication process so it increase the speed of the arithmetic operation. Adders and multipliers there is still potential for improvement in the synthesis of more complex data paths. In order to achieve that goal to levels have to be addressed. First, more sophisticated partitioning of the complex data path and more arithmetic optimization have to be applied. second, data path generators have to become more advanced and flexible in order to efficiently implement the more complex data path partitioning in a sum modified booth technique. Modern applications comprise several floating point operations, among them addition, multiplication, division and square root. We evaluate the performance of the S-MB technique have been used to provide accurate measurements of area utilization, critical path delay and power dissipation regarding various bit-width of the input numbers.

II. CONCEPT OF MODIFIED BOOTH ALGORITHM

The sign bit MB recoder which transforms redundant binary inputs to their MB recoding form. It proposes a two stage recoder which converts a number in modified booth representation. The first stage that converts carry save form of the inputs into signed digit form which is recorded in the second stage. So it matches the form which the MB digit request. This technique used high performance flexible coprocessor architecture targeting the computationally present an optimized design which reduce the area and power consumption. The direct recoding of the sum of two numbers is more efficient implementation of the FAM Fused Add Multiply unit compared to the conventional design. The efficient design of the FAM unit achieve the optimization of the recoding technique for direct MB form of the sum of two input numbers. The Sum Modified Booth (SMB) algorithm can be modified and applied either in signed or unsigned number which comprise of odd or even number of bits. There are three SMB technique used in the signed bit full adders and half adders as building block. Industrial tools for power estimation have been used to the correct measurements of the area utilization and power dissipation in different bit width of the input numbers. A Wallace tree is an efficient hardware implementation of the digital circuits that multiplies two integers. The carry signal to be propagate inside the adder, the critical path depends on the bit width of the inputs.

We focus on AM units which implement the operation The conventional design of the AM operator requires that its inputs and are first driven to an adder and then the input and the sum are driven to a multiplier in order to get. The drawback of using an adder is that it inserts a significant delay in the critical path of the AM. As there are carry signals to be propagated inside the adder, the critical path depends on the bit-width of the inputs. In order to decrease this delay, a Carry-Look-Ahead (CLA) adder can be used which, however, increases the area occupation and power dissipation.

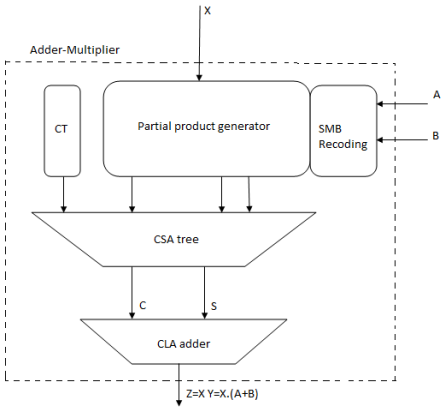


Fig.1. Fused design with the Direct Recoding of the sum of A and B

An optimized design of the AM operator is based on the fusion of the adder and the MB encoding unit into a single data path block by direct recoding of the sum to its MB representation The Fused Add-Multiply (FAM) component contains only one adder at the end (final adder of the parallel multiplier). As a result, significant area savings are observed and the critical path delay of the recoding process is reduced and decoupled from the bit-width of its inputs.

In this work, we present a new technique for direct recoding of two numbers in the MB representation of their sum.

Equation describes the generation of the partial products:

$PP_j=X.Y_j^{MB} = \bar{p}_{j,n}2^n+\sum_{i=0}^{n-1} p_{j,i}.2^i$ ...(1)

The partial products are generated, they are added, properly weighted, through aWallace Carry-Save Adder (CSA) tree along with the Correction Term (CT) which is given by the following equations:

CT=CT(low)+CT(high) ....(2)

The carry-save output of the Wallace CSA tree is leaded to a fast Carry Look Ahead (CLA) adder to form the final result.

$Z=X.Y=CT\sum_{j=0}^{k-1} PP_j.2^{2j}$ ....(3)

Optimized solutions for the FAM design enabling the targeted operator to be timing functional (notiming violations) for a larger range of frequencies. The proposed designs deliver improvementsin both area occupation and power consumption.

When we form the Most Significant Digit (MSD) of the S-MB recoding scheme, we distinguish two cases: In the first case, the bit-width of A and B is even, while in the second case, both A and B comprise of odd number of bits

$Y_j^{MB} = -2s_{2j+1}+ s_{2j+} c_{2j}$ ....(4)

In this scheme that using two full adders critical path delay of *S-MB*1 recoding scheme is constant in respect to the input bit-width and is given by the equation:

$T_{S\text{-}MB1}=T_{FA,Carry}+T_{FA^*,Sum}$ .....(5)

The second approach The second approach we consider the initial values $c_{0,1}=0$ and $c_{0,2}=0$.There will be a half adder used replaced in the full adder.

$T_{S\text{-}MB2}=T_{HA,Carry}+T_{FA,carry}+T_{HA^*,Sum}$ ....(6)

The third scheme is consider that $c_{0,1}=0$ and $c_{0,2}=0$ We build the digits based on s_{2j+1}, s_{2j}, $c_{2j,2}$

$T_{S\text{-}MB3}=T_{HA^*,Carry}+T_{FA,carry}+T_{HA^*,Sum}$ .....(7)

III. PROPOSED SYSTEM USING SQRT CSLA ADDER

The square-root carry select adder is constructed by equalizing the delay through two carry chains and the block multiplexer signal from previous stage. It is also called as non-linear carry select adder. The basic square-root Carry Select adder has a dual ripple carry adder with 2:1 multiplexer, the main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. From the structure of regular SQRT CSLA, there is scope for reducing delay and area utilization. The carry out is calculated from the last stage; in this the selection is done by using a multiplexer. An area-efficient carry select adder by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional carry select adder. That saves many transistor count and achieves the low power . SQRT CSLA design implemented with significantly less delay than a single stage CSLA of same size.

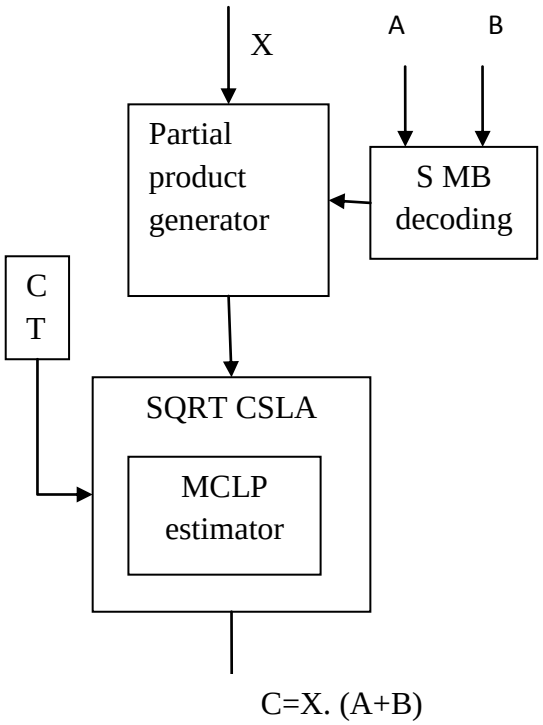
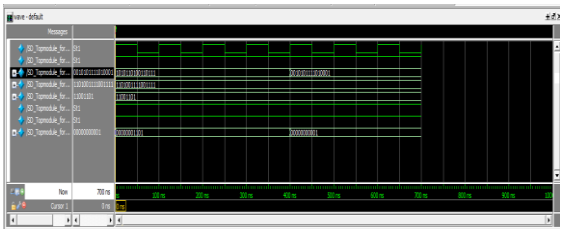


Fig. 2. FAM design using SQRT CSLA adder.

MLCP ESTIMATOR

The MLCP method produces a closed form with various bit widths *L* and column information *w*; thus, the compensated circuit can be established quickly, and the accuracy can be adjusted by Changing *w*. The proposed MLCP generates estimates by employing all nonzero code, which demonstrates high levels of inter correlation. Although MLCP method has higher complexity to estimate truncation errors when compared with ACPE one, According to the trade-off between accuracy and circuit area the MLCP method provides a balance between accuracy and circuit area. The proposed MLCP techniques achieves low-cost high accuracy Performance.

IV.OUTPUT OF THE EXISTING SYSTEM

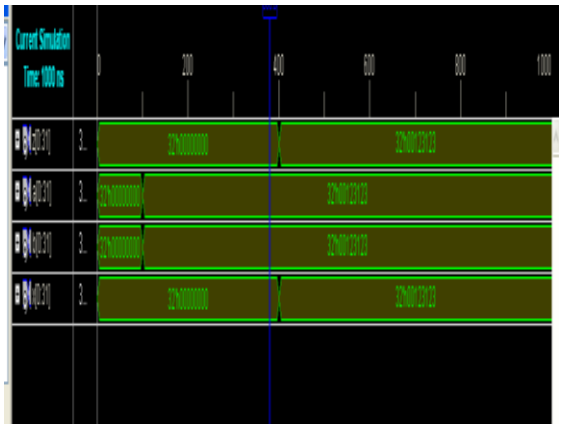


Three inputs are A, B, X. The output Y is generated by using multiplication of X and Y (Z=X.Y). Y denotes the addition of A and B. The final result denotes the combination of addition and multiplication that is Z=X.(A+B). Here 16 bits binary values are given as input. Carry inputs are used to generate the required output values.

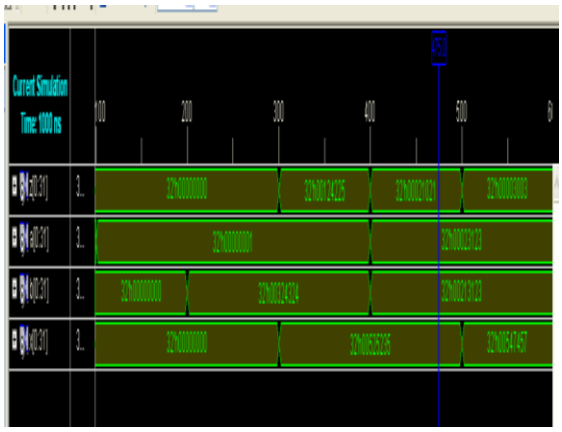
V. EXPERIMENT RESULTS OF EXISTING AND PROPOSED SYSTEM

Compared to previous methods, combination of MLCP and SQRT CSLA provides a maximum result. It reduces the power consumption, area covered by the chip and time delay of the process.

MP3



MP2



MP1

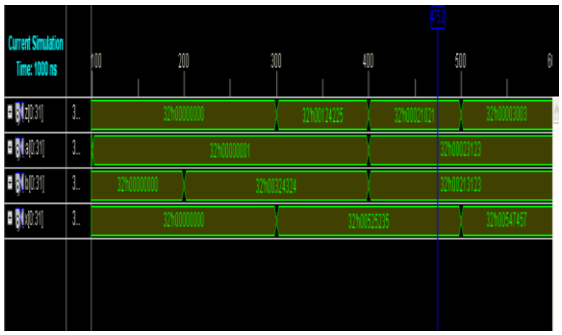


Table. 1. Comparision of existing and proposed results.

Methods	Area(um^2)	P(mW)
CSA	39284	34
SQRT,CSLA, MLCP	33567	26

RESULTS FOR DELAY:

- Delay of MB1=5.357687
- Delay of MB2=5.303979
- Delay of MB3=5.360615

VI. CONCLUSION

We propose a structured technique for the direct recoding of the sum of two numbers to its MB form. We explore three alternative designs of the proposed *S-MB* recorder and compare them to the existing ones. The proposed recoding schemes, when they are incorporated in FAM designs, yield considerable performance improvements in comparison with the most efficient recoding schemes found in literature. In addition, in all cases there is at least one FAM design that incorporates a proposed recoding scheme and outperforms both levels. The corresponding figures for odd bit-width are omitted as the results of comparison for both area and power consumption metrics are similar to the ones for even bit-width. This brief presents a closed MLCP formula that includes column information *w* to adjust accuracy depending on system requirements. This formula is derived without performing time-consuming and exhaustive simulations, and can be applied to lengthy Booth multipliers to achieve high-accuracy performance. Therefore, the proposed MLCP compensated circuit can be used to develop a high-accuracy, low-cost, and flexible fixed-width Booth multiplier.

REFERENCES

[1] Alberto Garc´ıa, Lukusa D. Kabulepa, Manfred Glesner"Efficient Estimation of Signal Transition Activity in MAC Architectures"Institute of Microelectronic SystemsDarmstadt University of TechnologyKarlstrasse 15, Darmstadt, D64283Germany

[2]. A. Amaricai, M. Vladutiu, and O. Boncalo, "Design issues and implementationsfor floating-point divide-add fused," IEEE Trans. Circuits Syst. II–Exp. Briefs, vol. 57, no. 4, pp. 295–299, Apr. 2010.

[3] Earl E. Swartzlander Jr., Life Fellow, IEEE, and Hani H.M. Saleh,"FFT Implementation with Fused Floating-Point Operations"IEEE transactions on computers, vol. 61, no. 2, February 2012

[4] S.Nikolaidis, E. Karaolis, and E. D. Kyriakis-Bitzaros, "Estimation ofsignal transition activity in FIR filters implemented by a MAC architecture,"IEEE Trans. Comput.-Aided Des.Integr. Circuits Syst., vol.19, no. 1, pp. 164–169, Jan. 2000.

[5] Reto Zimmermann and David Q. Tran DesignWare, Solutions Group, Synopsys, Inc. 2025 NW Cornelius Pass Rd., Hillsboro, OR 97124 "Optimized Synthesis of Sum-of-Products" Proceedings 37th Asilomar Conference on Signals, Systems, and Computers, November 2003

[6] P.Sasi Bala & S.Raghavendra Digital Electronics & Communication, Chaitanya Engineering College, Vishakapatnam(A.P), India"A New VLSI Architecture of Parallel Multiplier–AccumulatorBased on Radix-2 Modified Booth Algorithm" International Journal of Instrumentation, Control and Automation (IJICA) ISSN : 2231-1890 Volume-1, Issue-2, 2011

[7] Vamsi Krishna Pedarla (M.Tech), P.Nagaraju (M.Tech) "Modified Covalent Redundant Binary Booth Encoding For Fast 64*64 Multiplier Design" International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 3, May-Jun 2012

[8] K.N.Varaprasad, Dr.Nisha Sarwade and Ch. M Krishna"Low Power Multiplier-Accumulator" International Journal of Emerging Trends in Electrical and Electronics (IJETEE) Vol. 2, Issue. 2, April-2013

[9] W.-C. Yeh and C.-W. Jen, "High-speed and low-power split-radixFFT," IEEE Trans. Signal Process., vol. 51, no. 3, pp. 864–874, Mar.2003.