International Journal of Engineering Research-Online
A Peer Reviewed International Journal
Articles available online http://www.ijoer.in

Vol.3., Issue.3, 2015

RESEARCH ARTICLE

ISSN: 2321-7758

High Gain Low Power GPS RF Frontend LNA Design and Optimization Using 0.18µm CMOS

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Article Received: 30/04/2015 | Article Revised on:06/05/2015 | Article Accepted on:10/05/2015

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ABSTRACT

The design of a Low Noise Amplifier (LNA) in Radio Frequency (RF) circuit requires the trade-off many importance characteristics such as gain, Noise Figure (NF), stability, power consumption and complexity. In this paper the aim is to design and simulate a single stage LNA circuit with high gain and low noise using MOSFET (NMOS) for frequency 1.575 GHz. A single ended LNA has successfully designed with High forward gain and Law noise figure at the frequency of 1.575 GHz.

Key Words— Low Noise Amplifier, Noise Figure, Gain, CMOS, GPS Frequency.

I. INTRODUCTION

Communication technology is moving toward a major mile one. The explosive growth of the wireless industry, global access to the internet, and the ever increasing demand for high speed data communication are spurring us toward rapid developments in communication technology. Wireless communication plays an essential role in this transformation to the next generation of communication system. Cellular phones, pagers, wireless local area networks, global positioning system (GPS) handhelds, and short-range data communication devices employing Bluetooth and ultra wideband technologies are all examples of portable wireless communication devices. Nowadays, driven by insatiable commercial demand for low cost and low power multi-standard portable devices, RF designers are urged to develop new methodologies that allow the design of such products [4].

An irreplaceable component of any RF receiver is the front-end low-noise amplifier (LNA). As the first active building block in the receiver front-end, the LNA should provide considerable gain while minimizing the noise introduced to the system. Figure-1 depicts the simplified structure of an RF receiver [6].

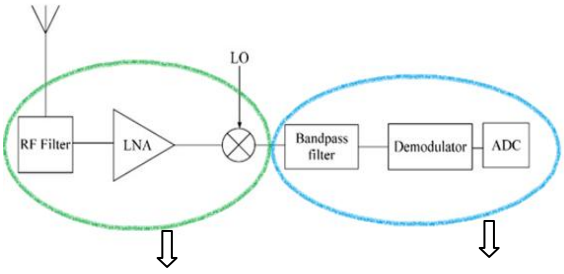


Figure:-1 - Block diagram of a simplified RF receiver

where almost any two of six parameters trade with each other to some extent. The radio frequency signal received at the antenna is weak. Therefore, an amplifier with a high gain and good noise performance is needed to amplify this signal before it can be fed to other parts of the receiver. Such an amplifier is referred to as a Low Noise Amplifier and

forms an essential component of any RF integrated circuit receiver. The total noise performance of the receiver depends on the Gain and Noise Figure of the LNA. The trade-offs involved in the design of such circuits can be summarized in the "RF design hexagon" shown in Figure-2.

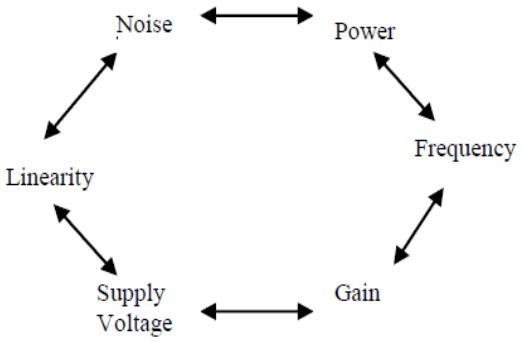


Figure:-2 RF Design Hexagon

II. TARGET SPECIFICATIONS

For the designing of a low noise amplifier (LNA) it seems appropriate to establish what the target specifications are. This is done in terms of a number of various parameters.

1. Noise Performance

The fundamental noise performance parameter is the Noise Factor (F), which is defined as the ratio of the total output noise power to the output noise due to input source. If the Noise Factor is expressed in decibels it is called the Noise Figure (NF). Another related and often talked about parameter in RF applications is the Signal-to-Noise Ratio (SNR), which is the ratio of the signal power and the noise power

NF = 10 log F

$SNR = P_{signal} / P_{noise}$

$F = (P_{si} / P_{Ni}) / (P_{so} / P_{No}) = 1 + Te/Ts$

2. S-Parameters

To represent a two-port network at microwave frequencies, scattering parameters (Sparameters) can be used. S-parameters themselves (S11, S12, S21, S22) represent reflection and transmission coefficients of the two-port under certain "matched" conditions.

$S_{11} = b_1(I_1) / a_1(I_1)$ and $a_2(I_2) = 0$ (input reflection coefficient; output port matched)

$S_{21} = b_2(I_2) / a_1(I_1)$ and $a_2(I_2) = 0$ (forward transmission coefficient; output port matched)

$S_{22} = b_2(I_2) / a_2(I_2)$ and $a_1(I_1) = 0$ (input reflection coefficient; input port matched)

$S_{12} = b_1(I_1) / a_2(I_2)$ and $a_1(I_1) = 0$(reverse transmission coefficient; input port matched)

3. Gain

The gain of the device is its ability to amplify the amplitude or the power of the input signal. It is defined as the ratio of the output to the input signal and is often referred to in terms of decibels.

$Voltage\ gain$ = 20 (Vout/Vin)

Power gain is generally defined as the ratio of the power actually delivered to the load to the power actually delivered by the source.

4. Stability

In the presence of feedback paths from the output to the input, the circuit might become unstable for certain combinations of source and load impedances. An LNA design that is normally stable might oscillate at the extremes of the manufacturing or voltage variations, and perhaps at unexpectedly high or low frequencies. The stability factor is given as in Equation

$K = \{1+|\Delta|^2 - |S_{11}|^2 - |S_{22}|^2\} / \{2|S_{11}||S_{22}|\}$

$\Delta = S_{11}S_{22} - S_{12}S_{21}$

When $K > 1$ and $\Delta < 1$, the circuit is unconditionally stable.

5. Design Target

Based on the preliminary studies of LNA, the design target for low noise amplifier is specified in the Table-1.

Parameter	Specification	Units
	Single-ended LNA	
Frequency	1.575	GHz
Noise Figure	< 3	dB
Power Gain(S21)	>10	dB
S11	<-10	dB
S12	<-10	dB
Power consumption	5-10	mW
Source/load impedance	50	Ohm
Power supply	1.8	V
Current	<5	mA
Technology	CMOS 0.18 µm	µm

Table:-1 -LNA specifications design target.

III. SINGLE-ENDED LNA DESIGN

The topology chosen is a single-ended LNA. It employs inductive source degeneration (inductor L_S connected to the source of transistor M1). This method has the advantage that one has a greater

control over the value of the real part of the input impedance through the choice of inductance. Cascoding transistor M2 is used to reduce the interaction of the tuned output with the tuned input. The RF input is coupled to the gate of the amplifier by the coupling capacitance C0. Transistor M3 is the biasing transistor and forms a current mirror with transistor M1. The width of M3 is kept a small fraction of the width of M1 to minimize the power overhead of the bias circuit. Output Inductor, L_d resonates with output load to maximize output power transfer and gain at resonance frequency. The width of the cascoded transistor must be sized to trade-off common source gain reduction and increase of parasitic source capacitance of M2 (both are consequence of a wider M2). Cascode transistor helps to reduce S21 and reduce *Cgd1* Miller effect. Rbias is large enough so that its equivalent current noise is small enough to be ignored. Lg is used to set the resonant frequency.

BASIC STEPS AND CALCULATION

The design procedure followed by me for the design of single-ended LNA is Power optimization based. The input impedance for the single stage LNA design is:

$R_{in} = R_g + (L_s*g_m)/C_{gs} + j(wL_s – 1/wC_{gs})$

It can be written as,

$R_{in} = R_g + R_G + j (X_{LS} - X_{CGS})$

Where,

$R_a = (L_s*g_m)/ C_{gs}$

Therefore, the impedance of the MOSFET without feedback is:

Rin = Rg - jXCGS → Rin = - jXCGS

Adding series feedback adds the Ra + jX_{LS} term to the original input impedance. Additionally, another inductor is added in series with the gate Lg that is selected to resonate with the Cgs Capacitor. The Input resistance (Rin) achieved is: Rin = $(L_s*g_m)/ C_{gs}$. Where Rin may be say 50 ohms. Lg is designed so that at the resonant frequency it cancels out Cgs i.e $j(wL_s – 1/wC_{gs})$. In most LNA designs the value of Ls is picked and the values of gm and Cgs are calculated to give the required Rin. The design steps followed by me for the design of single-ended low noise amplifier are given below:

1.Find the optimum device width: The optimal value of Q in case of power optimization technique is:

$$Q_{L,opi,PD} = |C|(5\gamma/\delta)[1+(3/|C|)*(1+ \delta/5\gamma)]$$

= 3.9

Where, γ = 2, δ = 4, α =.85. The equation for the device (M1) width is

$$W_{M1},t\ ,PD = 3 / 2Cox\ LQ_{L,opt\ ,P\ D}RS\ _{\omega 0}$$

The operating frequency (f0) is 1.575GHz and ω0=2*3.14*1.575G= **9.891Grps**. The value of R_S is 50Ω.

For 0.18 µm technology,

µn =332.1 c.m2/v/s, Cox=8.221 10-15F/ μm^2, µnCox=273.03µ, L=.18 µm,

So, $W_{M1,t\ ,PD}$=**525.56 µm**.

2. Find CGS(Gate-Source capacitance):

We know,

$$C_{gs1} = (2/3)*Cox * W_{M1}* Lmin$$

So, $C_{gs1} = (2/3)* 8.221* 10^{-15} *525.56*0.18$

= **0.518 PF**

3. Find the device transconductance (g_{M1})

$$g_{M1}= √2*µ_n *C_0 *(W/L)\ M_1* I_DM1$$

I take $IDM1$= 5 mA.

So, g_{M1}=**89.27 mA/V**.

4. Find the transistor unity gain frequency (ωT)

$$\omega_T = g_{M1\ /}\ C_{gs1}$$

= **172.336 *Grps***

5. Expected noise figure $Fmin$,: The expected noise figure can be computed by below formula:

$$F_{min} \approx 1 + 2.4(\gamma/\alpha)*(\omega_0/\omega_T) \geq 1 + 1.62(\omega_0/\omega_T)$$

Where, γ =2 and α=1

So, F_{min} ≈ **0.3858 dB**

When ID increase then ωT increase and NF decreases at the expense of more power.

6. Starting value of Degeneration Inductor LS:

The value of this inductor is fairly arbitrary but is ultimately limited on the maximum size of inductance allowed by the technology, which is typically about 10nH.

$$Rs = g_m *L_S / C_{gs} = \omega_T L_S$$

So, $L_S = R_{S\ /}w_T$

=**0.29 nH**.

7. Evaluation of Lg:

We know,

$Lg = 1/(W_0^2*C_{gs}) – Ls$

So, Lg =**19.7 nH**.

8. Evaluation of Ld:

Here the value of C_L=1 pF

$$L_d = 1/(W_0^2*C_L)$$

So, L_d = **10.22 nH**.

9. Width of transistors: Size of M3 is chosen to minimize power consumption. So W_{M3} =60 µm. size of M1 = M2, So that they can have shared drain area. It can reduce the impedance looking into gate and drain of M1 degrading the input match and noise performance, so both transistors sizes are to made equal. Transistor M2 is used to reduce the miller effect.

10. Value of bias resistor:

Rbias must be large enough so that it‟s equivalent current noise can be neglected. So,

Rbias=2KΩ.

11. Calculation of power dissipation (Pd) :

We know, $Pd = Vdd * ID$

So, Pd = 1.8 * 5 * 10^{-3}= **9 mW**.

IV. SCHEMATIC AND SIMULATION RESULTS:

Using the library TSMC_RF_CMOS for 0.18µm technology in Advance System Design, the schematic of single ended LNA on ADS schematic editor tool was created as shown in Figure-3. The simulation includes DC simulation, S-parameter simulation, Pnoise. From DC simulation the power consumption is got. The transistors operation points are optimized from DC simulation. It is important to give the larger gain for LNA design with the optimum operation point.

The various simulation iterations are performed on the proposed LNA circuit to meet design requirements.

Schematic of single ended LNA: Figure:-3 shows the schematic of single-ended LNA on Advanced Design System tool.

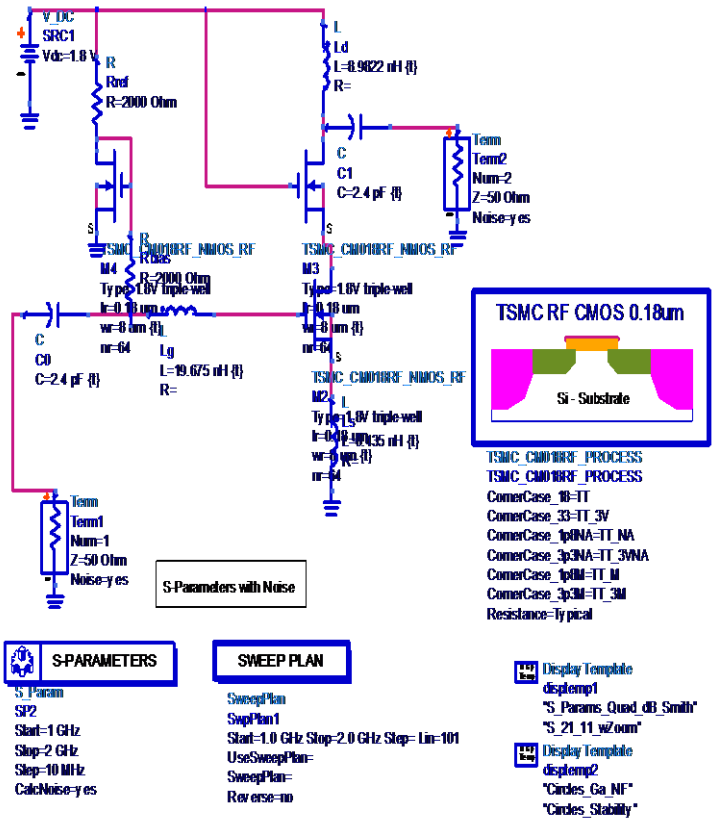


Figure:-3: Schematic of Single-Ended LNA.

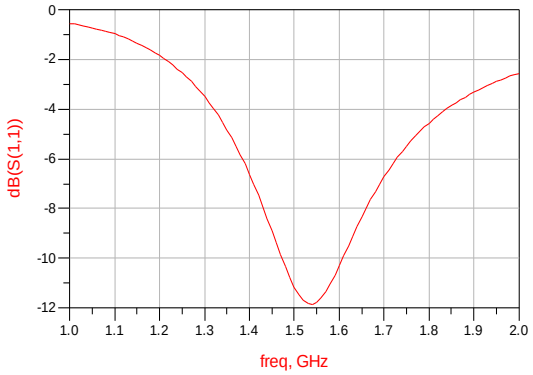
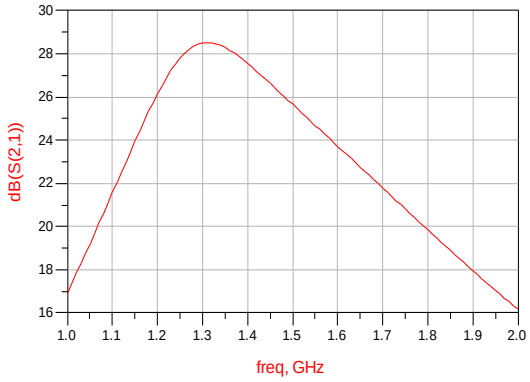


Figure-4(a): S11 plot for Single Ended LNA



. Figure-4(b): S21 plot for Single Ended LNA.

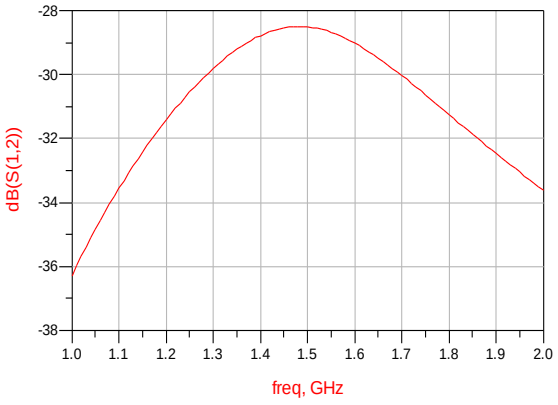


Figure-4(c): S12 plot for Single Ended LNA

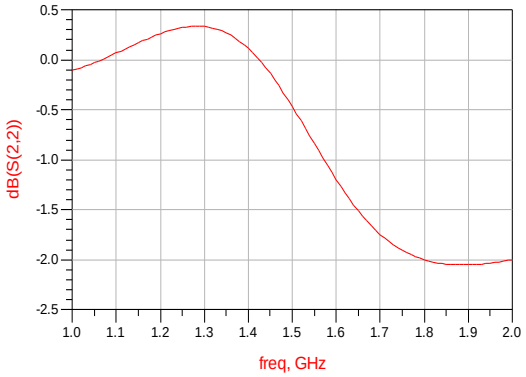


Figure-4(d) S22 plot for Single Ended LNA

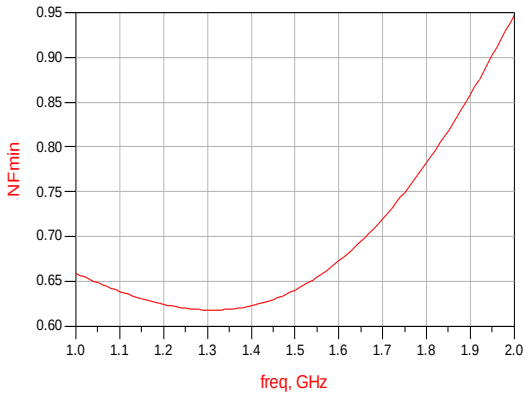
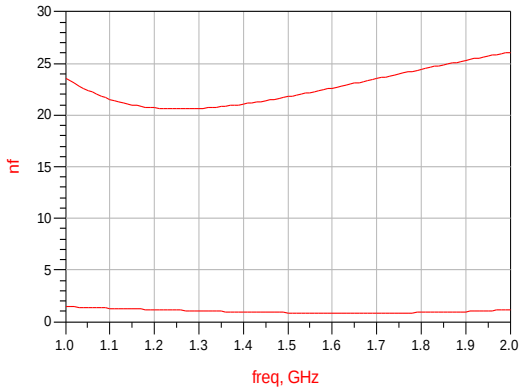


Figure-4(e): NFmin plot for Single Ended LNA



. Figure-4(f): NF plot for Single Ended LNA

The simulation results of single-ended LNA achieved at the typical process are summarized in the Table-2.

Performance Parameter	Value	Unit
Noise Figure (NFmin)	0.68	dB
Noise Figure (NF)	1.092	dB
Power Gain (S21)	25	dB
S22	-1	dB
S11	-12	dB
S12	-29	dB
ID	5	mA
Power consumption	9	mW

Table-2: Performance parameters of the Single Ended LNA (RF frequency 1.575GHz)

V.CONCLUSION:

This work is an effort towards rigorous comparative analysis with an aim to design a low noise RF amplifier with a high figure of merit. The target specifications at the start of the design having 1.575 GHz operating frequency, gain of more than 15dB and maximum noise figure 3dB. The corresponding values obtained by simulating Single Ended LNA topologies have been reported and it was found that the design using Single Ended LNA topologie approximated the target specifications reasonably well. This circuit simulate on the Advanced Design System and saw the resule of the S-parameters, Gain and Noise Figure.

Acknowledgements:

It is my great pleasures to express gratitude to the people who have been instrumental in the successful completion of this work. First I would like to convey my sincere thanks to my guide Prof. Hasmukh Koringa, GEC Rajkot and Prof. Deepak Parashar, GCET for his exemplary guidance, monitor and constant encouragement throughout the course of this work.

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