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REVIEW ARTICLE

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FPGA IMPLEMENTATION OF PULSE SHAPING FIR INTERPOLATION FILTER FOR MULTI-STANDARD DUC

SNEHA R[1], SUGANYA P[2]
[1,2]Department of Electronics and Communication Engineering,
T.R.P Engineering College (SRM Group)
Tiruchirappalli, Tamil Nadu, India.

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SNEHA R

ABSTRACT

A two-step optimisation techniques to design a reconfigurable VLSI architecture of an interpolation filter for multi-standard Digital Up Convertor (DUC) is proposed in this brief. First technique initially implements the reduction of multiplication per input samples and addition pre input samples by designing a root raised cosine filter for multi-standard DUC. In the second technique we use 2 bit binary common sub expression based BCS elimination algorithm to design an efficient constant multiplier, which is the basic element of any filter .In the second techniques we use booth multiplier to generate partial product instead of shift and add method to reduce further area These two techniques have succeeded in reducing the area and power consumption and thus improving the operating frequency.

Key Words- Finite impulse response (FIR), Software defined radio (SDR) system, Root Raised cosine filter (RRC), Digital Up Convertor (DUC).

I. INTRODUCTION

Finite Impulse Response (FIR) filters play a vital role in many signal processing applications in communication systems. Many task such as spectral shaping, matched filtering, interference cancellation, channel equalization, etc. can be performed with the use of FIR filters. A single device that supports all the standards under wireless communication is referred to as Software Defined Radio (SDR) [1]. Finite impulse response (FIR) filters are employed as channel filters in SDR receivers. The basic idea behind the SDR is to replace most of the analog signal processing in the transceiver side with digital signal processing in order to provide the advantage of flexibility through reconfiguration. This helps different air- interfaces to be implemented on a single hardware platform to support multi standard wireless communication. The reconfigurability of the receiver to work with different wireless communication standard is another key requirement in a SDR [2]. In order to reduce the complexity of the design we use the interpolation FIR filter [3].

Several designs have been proposed to design a low power consumption and low area and low complexity design reconfigurable FIR filter for SDR system. A modified canonical signed digit (CSD) [4] is proposed to design to improve power consumption but this have been obtained by the reduction of operating speed and this technique is unsuitable for SDR system. Low power and low area FIR filter has been achieved by using the efficient Look Up Table (LUT) but however this design is not applicable for higher order filter because it increases the size of

ROM. A Distributed Arithmetic (DA) [5] has been proposed to design an area-delay-power efficient filter. Logic depth is defined as number of addition operation required to perform multiplication, it is also known as critical path. An algorithm based on binary common sub-expression [6] elimination as been proposed this proposed design consumes less power and area but this involves the addition adder block which makes the design unfit for SDR system.

In order to overcome the above mentioned disadvantage a new reconfigurable pulse shaping FIR interpolation filter for multi-standard DUC has been proposed. This technique performs two optimization functions, initially it reduces the no of addition per input sample and multiplication per input sample and another is that to design an efficient multiplier with the help of 2- bit binary common sub-expression.

II. Design of Root raised cosine FIR filter

To design a multi-standard DUC we consider three different standards such as digital video broadcasting, Wideband code division multiple access Universal mobile telecommunication system. The above mentioned are designed using root raised cosine filter [7] as pulse shaping filter for it can reduce the inter symbol interference and also decrease the bit error rate. The given standards and its specification are calculated using MATLAB and in the proposed architecture we use 4, 6 and 8 interpolation factor and their corresponding tap filter such as 25, 37 and 49 tap filter.

To design and implement RRC filter with the above specification we need to face the following challenges.

1) It is noted that the number of multipliers and adder count increase with the increase in filter parameters for designing filter. As the no of multipliers and adders increases the power and area consumption also increase linearly.

2) The most recently proposed method to design an efficient multiplier is the binary common sub-expression (BCSE) algorithm. It is know that by choosing proper length of BCS we can reduce hardware usage. The propagation delay of the design is measured by computation time of (LD+1) addition operation. By using the BCS algorithm we can reduced the logic depth thereby we can increasing the operating frequency of filter.

III. SOLUTION FOR PROPOSED DESIGN

The two following steps have been given to solve problem for the proposed system.

1) The function of first coding pass (FCP) block, coefficient sets of two RRC filter of same length but which differ only by filter parameter are passed through 2:1 multiplexer, here we use one control parameter (FLT_SEL) to select the desired filter which the roll off factor. This technique reduces 50% of total coefficients.

2) Similarly in the second coding pass (SCP) the output of the FCP block as fed as the input. These inputs are allowed to pass through to another set of multiplexer; here we use one control parameter (INTP_SEL) which is used to select the desired filter depending on interpolation filter. This technique further reduces the total coefficients. From the proposed technique we know as we use different filters with different specification we can reduces MIPS and AIPS.

3) In the given 2-bit BCS based BCSE technique the logic depth is given by the equation as shown below

$$LD_{2BCS} = [\log_2 2] + \log_2 [16/2] = 4 \quad (1)$$

here $\log_2 2$ is the 2-bit BCS term and $\log_2 [16/2]$ is the word length is 16 bits.

The propagation delay is also given as follows

$$T_{2BCS} = 4*t_{add} + t_{4:1\ mux} + t_{acc} \quad (2)$$

Here t_{add} is delay in adder, $t_{4:1\ mux}$ is the delay in the 4:1 multiplexer, t_{acc} is the delay in the final adder.

IV. RECONFIGURABLE RRC FILTER ARCHITECTURE

The block diagram for the proposed reconfigurable architecture of FIR interpolation filter is shown in Fig. 1. In the proposed block, two filter parameters namely INTP_SEL and FLT_SEL is used to select different interpolation factor and roll factor, respectively. In the proposed design, four clock signals act as input to the design.CLK is the master clock signal used in the design and used to sample the output RRCOUT which operates at higher rate. Three other signals that are derived from clock signals namely CLK4, CLK6 and CLK8 are used to sample the input data RRCIN for different interpolation factor. The major blocks present in the reconfigurable RRC Filter consists of data generator (DG), a coefficient generator (CG), a coefficient selector (CS) and the final accumulation unit (FA).

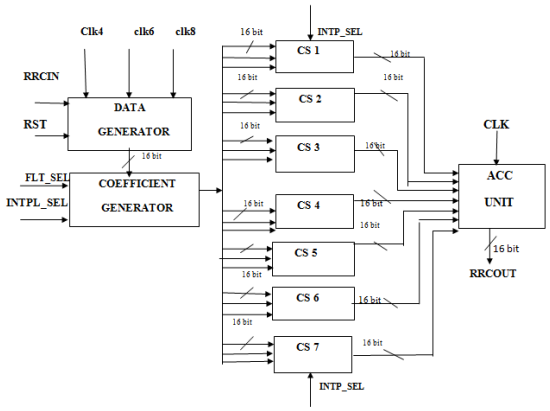

Fig. 1. Architecture for proposed reconfigurable RRC filter.

A. Data Generator (DG) Block.

Data generator block produces data according to the interpolation factor selection parameter. It is used to sample the input data RRCIN based on the selected interpolation factor (INTP_SEL). It is used as serial to parallel converter. From the design point it is observed that to implement 25, 37 and 49 tap filters with interpolation factor 4, 6 and 8 we constitute a branch of seven taps.

[25/4] = [37/6] = [49/8] = 7

Thus it is observed that to generate a full filter response we require seven sub filters for multiplication of filter coefficients with input sequence. A 7 bit shift register is used for serial to parallel conversion. Here three different 7- bit shift register is taken where the sample input has been sampled at three different sample clocks. Finally, interpolation selection parameter is used to select the sift register whose output is chosen to generate up sampled data's.

B. Coefficient Generator (CG) Block:

The purpose of Coefficient Generator block is to perform multiplication operation between the filter coefficients and the input sequence. The data flow diagram of the CG block is shown in Fig. 2. The below mentioned steps have been performed to ensure that the design enables low area consumption and complexity is reduced.

1) *FCP:*

The first block in the coefficient generator is the first coding pass .The inputs of the FCP block are two sets of 25, 37, and 49 taps filter coefficient which differs by roll off factor. In the FCP block, three coding block works in parallel condition for different interpolation factors. The function of FCP block is to find the matching between bits and code them vertically of same filter length. In the multiplexer unit the desired output is selected using selection line the output of final unit is added. The block for the FCP is as shown in Fig.3.

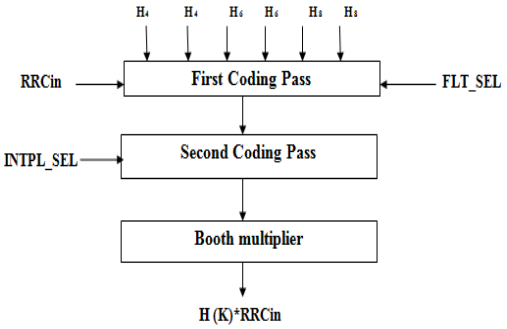

Fig. 2. Data flow diagram of coefficient generator.

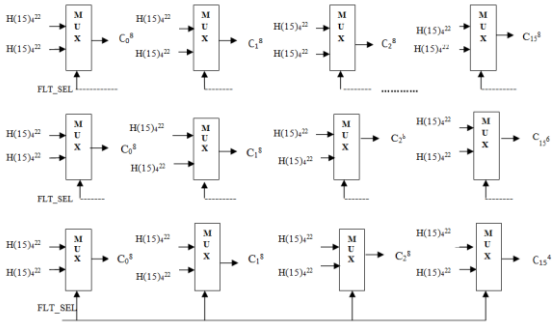

Fig. 3. Architecture of FCP Block.

2) *SCP:*

The three set of coded coefficients that are obtained from the first coding pass are 13, 19 and 25 and it is fed as input to second coding pass. These inputs are allowed to pass another CP block to obtain the final coefficients. The function of the SCP block is to explore the common term present vertically and code these coefficients and the output obtained is represented as S. INTP_SEL is used as the selection line in the SCP block. The architecture of the SCP block is given in fig. 4.

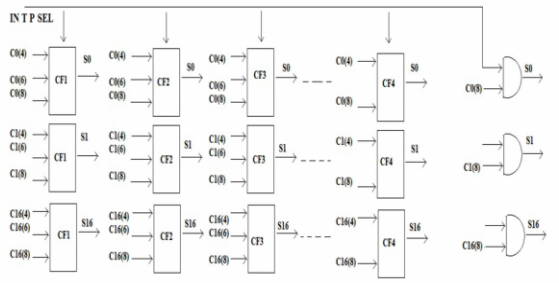

Fig. 4. Architecture of SCP Block.

3) Booth Multiplier:

Booth multiplication is a technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied. It is the standard technique used in chip design, and provides significant improvements over the "long multiplication" technique. It is possible to reduce the number of partial products by half, by using the technique of radix 4 Booth recoding. The basic idea is that, instead of shifting and adding for every column of the multiplier term and multiplying by 1 or 0, we only take every second column, and multiply by ±1, ±2, or 0, to obtain the same results.

The advantage of this method is the halving of the number of partial products. This is important in circuit design as it relates to the propagation delay in the running of the circuit, and the complexity and power consumption of its implementation. It is also important to note that there is comparatively little complexity penalty in multiplying by 0, 1 or 2. All that is needed is a multiplexer or equivalent, which has a delay time that is independent of the size of the inputs. Negating 2's complement numbers has the added complication of needing to add a "1" to the LSB, but this can be overcome by adding a single correction term with the necessary "1"s in the correct positions.

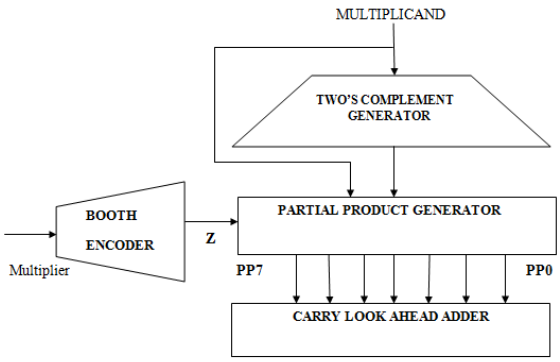

Fig .5 Architecture for booth multiplier

C. *Coefficient Selector* (CS):

The output of the CG block is given as the input to the coefficient selector block. The purpose of the coefficient selector is to select the proper data to the final accumulation unit depending on the interpolation factor. The hardware architecture of the CS block is shown in Fig.6.

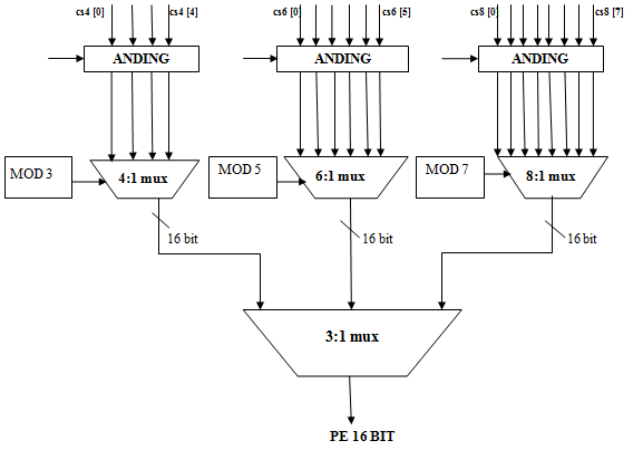

Fig.6 Architecture for coefficient selector block

D. *Final accumulation unit*:

Since there are six adders and register we require seven sub filter. In order to get the output without any delay we design the reconfigurable RRC filter based on the transposed direct form architecture.

V. IMPELMENTATION RESULTS

Detailed circuit design of reconfigurable RRC filter is implemented is described in behavioural level using the hardware description language, verilog. The design is implemented on Xilinx ISE 12.1. Code has been developed and is stimulated using ISE stimulator. The functional and timing waveform and the RTL schematic are carried out efficiently. Comparison has been made with the previous reconfigurable architecture which is implemented on the FPGA platform [8] and shows the usage and the gate count comparatively lower than the existing work. The 2-bit BCSE design consumes less power than that of the previously proposed 3-bit BCSE method. Power can be calculated in Xilinx using the X-power tool.

The utilization report dot the proposed design is given in table .1.

TABLE. 1. UTILIZATION REPORT FOR THE PROPOSED DESIGN.

Place and Route Report	Proposed Design
Target device	xc3s100e-5vq100
Number of slice	40 out of 1960
Number of 4 input LUT	40 out of 1,920
Equivalent gate count	2880

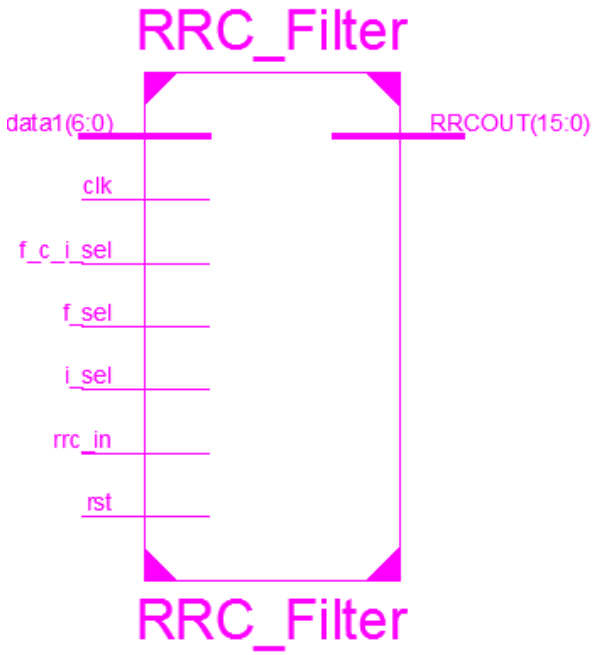

Fig. 9. RTL Schematic view

VI. CONCULSION

This brief describes about the problems in designing the reconfigurable FIR filter for multi-standard DUC, which is the important component in SDR system. It also provides the solution by giving two optimisation techniques to design filter with low area and power consumption and thereby increasing the operating frequency. The proposed design is more suitable for new reconfigurable multi-standard DUC of SDR system.

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