International Journal of Engineering Research-Online
A Peer Reviewed International Journal
Articles available online http://www.ijoer.in

Vol.3., Issue.3, 2015

RESEARCH ARTICLE

ISSN: 2321-7758

DELAY MEASUREMENT IN ANALOG SIGNAL BIST BY USING SAMPLING HEAD TECHNIQUE

N.MALA[1], B.KARTHIGA[2]

[1]PG Scholar,Department of ECE,Srinivasan Engineering college,Perambalur,Tamilnadu,India.

[2]Assistant professor, Department of ECE, Srinivasan Engineering college, Perambalur, Tamilnadu, India.

Article Received: 29/04/2015 | Article Revised on:04/05/2015 | Article Accepted on:07/05/2015

ABSTRACT

Analog BIST mainly presents for measuring on chip voltages. In BIST application we cannot directly measure the on-chip voltages. So, sampling head technique is used. Sampling head consists of pair of flip-flops and voltage-to-delay cells. Voltage-to-delay cell is used to convert the input voltage into delay. In the proposed work, the voltage to delay cell is reduced and D flip flop is replaced by the buffer. Therefore, the area and delay get reduced to 30%.

Keywords: Built-in self-test (BIST), over sampling ratio, quantization, sub sampling.

I.INTRODUCTION

A common problem in analog circuits is bias variation. Because, when the process variation is increasing , the power supply is to be reduced. A mixed signal IC design is a method, to measure analog voltages for testing and debugging purposes. The sampling head technique consists of analog input voltage presented all over the chip. Hence, at each node, the input voltage is measured. Therefore, the measurement circuitry occupies small area and it is simple to design. In analog/RF BIST architecture, if we permit maximum area, then we should concentrate on total cost reduction. In the proposed architecture, the dc voltages (of BIST sensors) of the test nodes are all tied together to a common bus and digitized centrally through Analog-to Digital Converter (ADC).

In the previous work, a BIST method is introduced in which BIST subsystem is embedded in a mobile broadcast video receiver in 65-nm CMOS technology. The Subsystem is designed to perform analog and RF Measurements [1].On chip oscilloscopes reduce error by using sampling process. Automatic test Pattern generation is also used. Here, Glitches and Crosstalk is produced. This error can be reduced by using sampling process [3]. Then, Bluetooth radio is fabricated in a 130-nm CMOS. This transceiver architecture is used in digital baseband application processor. .Voltage controlled oscillator and the phase frequency detector has been replaced with a digitally controlled Oscillator [7]. Next, Analog to digital converter is designed by using delay lines. The voltage comparator is to be used convert the input voltage into digital code by using delay lines [9].

II. SAMPLING HEAD TECHNIQUE

Sampling head consists of voltage-to-delay cells and D flip-flops. To measure a corresponding node voltage, the sub sampled signal pair is fed to delay measurement unit to measure the delay. A clock signal is routed serially to all the sampling heads, which is fed to both the delay cells in the

sampling head. The delay of one element of the pair is controlled by the analog voltage VA*i* and that of the other by a reference voltage *V*ref.

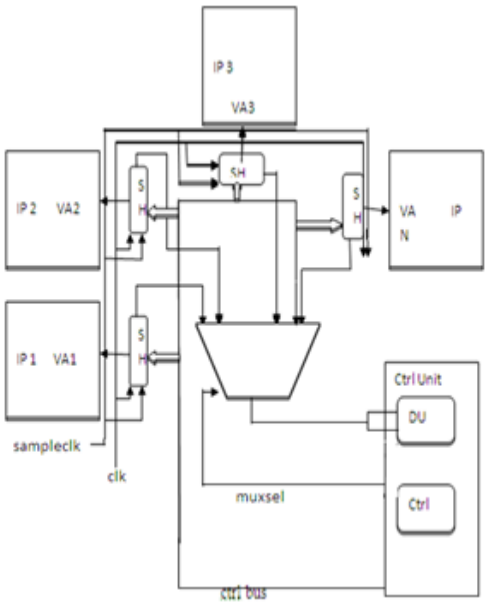

Figure1: Analog BIST architecture using sampling head technique

Thus, a voltage difference between the node voltage and reference shows up as a delay difference in the clocks at the output of the delay cell pair. To measure a certain test node, the corresponding sub sampled signal pair has to be fed to the delay measurement unit (DMU) with an appropriate select signal to the multiplexer.

III.PROPOSED WORK

The existing method has 13 voltage-to-delay cells and D flip-flops to maintain the delay. In the proposed work, the number of voltage-to-delay cells are reduced, and D flip-flop are replaced by buffer circuit, because buffer have the same operation as that of the flipflop . A buffer is one that provides electrical impedance transformation from one circuit to another. There are 2 types of buffer. Voltage buffer and current buffer. The difference between the flipflop and buffer is used to capture, or 'latch' the logic level which is present on the Data line when the clock input is high. The working of D flip flop is similar to the D latch except that the output of D Flip Flop takes the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is active low) and delays it by one clock cycle. Hence, it is commonly known as a delay flip flop.

D flip-flop occupy more area than the buffer circuit. So, buffer circuits are to be used in this architecture. The advantage of reducing voltage-to-delay cells is the area and delay gets minimized. Therefore, the critical path also gets reduced.

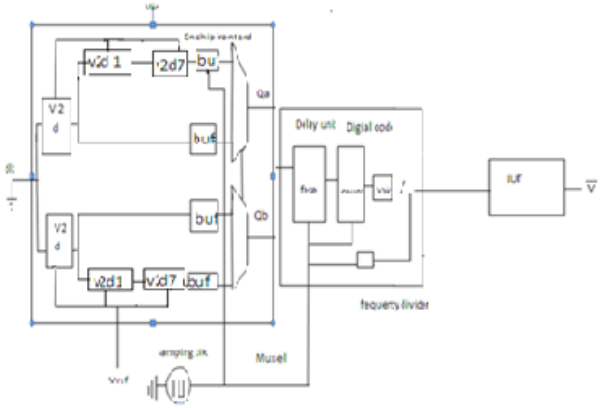

Figure2: Sampling head technique with reduced V2D cells

Implemented setup block diagram having a voltage -to-delay cells, and buffer circuits, and delay measurement unit. Each input node is connected to sampling head. Sampling head contain voltage-to-delay cells and buffer circuit.

III.EXPERIMENTAL RESULTS

Figure 3: Voltage To Delay Cell

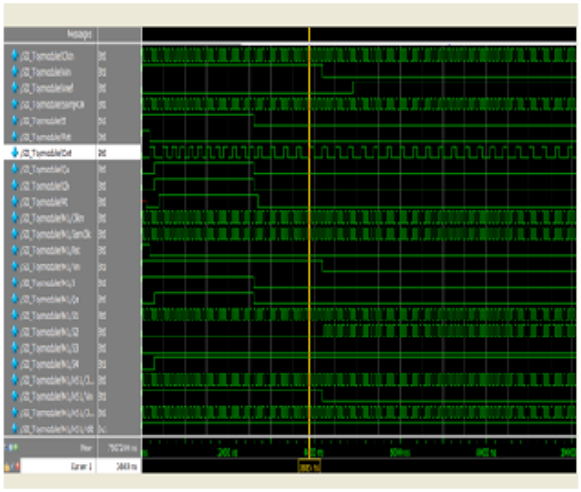

Figure 4: Sampling Head Technique Output

Simulation Result:

Table 1: Comparison Result

Voltage to delay cell	Delay	Number of gate counts
13	0.936ns	83
7	0.901ns	59

From the above tabular column, the delay and area get minimized by reducing the voltage to delay cell.

IV.CONCLUSION

This paper presents a sampling head technique which locally converting the test voltage into skew between a pair of sub sampled signals .This was achieved by sampling head placed at each node ,each sampling head consist of a pair of voltage controlled delay cells and pair of flip-flops. This approach reduces the routing of analog signals over long paths to the measurement unit, thereby saving the chip area. To measure a certain analog voltage the corresponding sub sampled signal pair is fed to delay measurement unit to measure the skew between this pair. In the proposed method, voltage to delay cells are further reduced and buffer is used instead of D flip flop. Hence, the 30% of delay and 37% of area can be reduced.

REFERENCES

[1]. B. Amrutur, P. K. Das, and R. Vasudevamurthy,(Dec 2011) '0.84 ps resolution clock skew measurement via subsampling,' *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 12, pp. 2267–2275, Dec. 2011.

[2]. G. Banerjee, M. Behera, M. A. Zeidan, R. Chen, and K. Barnett, (Sep 2011)'Analog/RFbuilt-in-self-test subsystem for a mobile broadcast video receiver in 65-nm CMOS,' *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1998–2008, Sep. 2011.

[3]. T. Hashida and M. Nagata,(Apr 2011) 'An on-chip waveform capturer and application to diagnosis of power delivery in SoC integration,' *IEEE J. Solid- State Circuits*, vol. 46, no. 4, pp. 789–796, Apr. 2011.

[4]. S.-K. Lee, S.-J. Park, H.-J. Park, and J.-Y. Sim,(Mar 2011) 'A 21 fJ/conversionstep 100 kS/s 10-bit ADC with a low-noise time-domain comparator for low-power sensor interface,' *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 651–659, Mar. 2011

[5]. G. Li, Y. M. Tousi, A. Hassibi, and E. Afshari,(Jun 2009) 'Delay-line-based analogto- digital converters,' *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 6, pp. 464–470, Jun. 2009.

[6]. R. B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, E. de Obaldia, and P. T. Balsara,(Dec 2004) 'Alldigital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS,' *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004

[7]. M. Z. Straayer and M. H. Perrott,(Apr 2008) 'A 12-bit, 10-MHz bandwidth, continuous-time $\sigma\delta$ ADC with a 5-bit, 950-MS/s VCO-based quantizer,' *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.

[8]. J. Xiao, A. V. Peterchev, J. Zhang, and S. R. Sanders,(Dec 2004) 'A 4-μa quiescent current dual-mode digitally controlled buck converter IC for cellular phone applications,' *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2342–2348, Dec. 2004.

[9]. Y. Zheng and K. L. Shepard,(Feb 2004) 'On-chip oscilloscopes for noninvasive time-domain measurement of waveforms in digital integrated circuits,' *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 3, pp. 336–344, Jun. 2003.

[10]. T. Watanabe, T. Mizuno, and Y. Makino,(Apr 2004) 'An all-digital analog-to-digital converter with 12μV/LSB using moving-average filtering,'*IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 38, no. 1, pp. 120–125, Apr. 2004.