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RESEARCH ARTICLE

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DESIGN A LOW POWER MICROPROCESSOR USING CLOCK GATING TECHNIQUE

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ABSTRACT

In today's era technology is scaling down rapidly and market demanding for the low power and high performance digital circuits like microprocessor. Scaling of supply voltage is limit the speed of the design and will lead to setup and hold time violation. Clock gating is effective technique which can be used to save 3 to 6% of total power. In this paper Microprocessor is implemented using Altera Quartus II tool and the logic of Clock gating is applying on datapath block. Total power dissipation is reduced by 20% of dynamic power.

Key Words— microprocessor, power, dynamic power dissipation, clock gating.

INTRODUCTION

As technology is shrinking and high performance is require, power dissipation is major issue for portable devices. Nowadays most of the devices are portable devices, so very low amount of power dissipation play major role in devices.

Power is an amount of energy consumed by devices per unit time[14]. Power is inversely proportional to the performance in term of speed. But for low power design, performance is bottleneck. So if power dissipation is less, performance will be increase.

Power dissipation means power which is dissipated in term of heat in devices[6]. There are two type of power dissipation in microprocessor. Those are Static and dynamic power dissipation. Static power can be known as leakage power, dynamic power is switching power as well as shirt circuit power[6].

For dynamic power dissipation there are two components one is switching power due to charging and discharging of load capacitance. The other is the short circuit power due to the nonzero rise and fall time of input waveforms. The switching power of a single gate can be expressed as[6]

$$P_D = \alpha C_L V_{DD}^2 f \qquad 1$$

Where α is the switching activity,
f is operation frequency,
C_L is the load capacitance,
V_{DD} is the supply voltage.

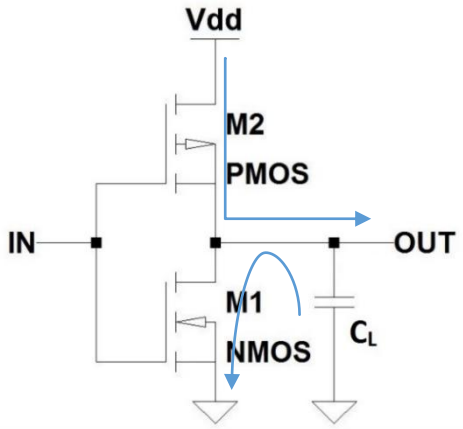

Figure 1 Dynamic Power dissipation[6]

Introduction of Microprocessor

It is controlling unit of portable devices, which is implemented on very small chip. It is a multipurpose, programmable device that accepts digital data as an input, processes it according to instructions stored in its memory, and provides results as output[13]. The basic block diagram of it is shown in below figure.

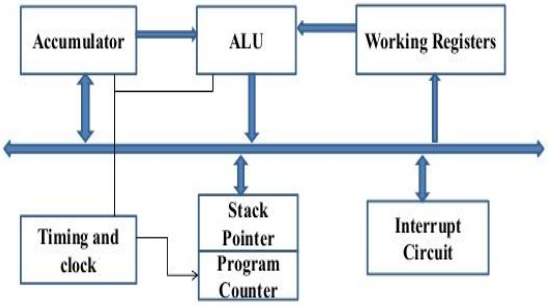

Figure 2 Block diagram of microprocessor[7]

Microprocessor has mainly four units[7],

- data path unit
- control unit
- machine unit
- interface unit

Clock Gating

Microprocessor is working on a clock, which is globally distributed in it. Clock play important role in microprocessor because this is the only component which is continuously switching[4]. So if we reduce the switching power of clock, we can also improve the power of microprocessor[11].

One signal is introduced here, that is clk-control signal. Clock gating means clock is ANDed with clk-control signal, when input data is in ideal stage[5]. Clock gating technique is mainly applied on sequential circuit, dynamic circuits[3][9].

For effective clock gating three things mainly considering[1],

1. Which circuit is gated?

If selected circuit is mostly active circuit, then it is worthless.

2. When circuits is gated?

In every circuit, one signal is taken place, which is known as predictor circuit. This is use for prediction, when input is arrived and when it becomes zero, so clock signal become gated over there.

3. How much period of time it will be gated?

Predictor circuit is take part for this too. It use for observation of input of gated circuit. When any input is assigned, then time period break and circuit run continuously.

Types of Clock Gating

Predictor circuit is design using two methods those are

- Latch free clock gating
- Latched clock gating

These both techniques have its own advantages and disadvantages. Let's start with latch free clock gating.

- Latch free clock gating

Clock gating is applied using different gates and latches. When clock is gated using gates like AND or OR gates, it is known as latch free clock gating[4]. But it has one disadvantage, glitch is generated over here. Glitch means unwanted signal, which is affect whole operation. For reducing the reducing the glitch effect OR gate must be work in active low region and AND gate is work in active high region.

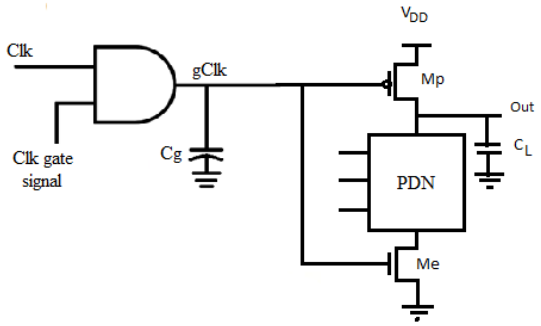

Figure 3 latch free clock gating[4]

- Latched clock gating

To overcome the disadvantage of latch free clock gating one new technique is introduced. In this technique, latches are used just before AND gate. Latch is working on positive edge of clock[3][12].

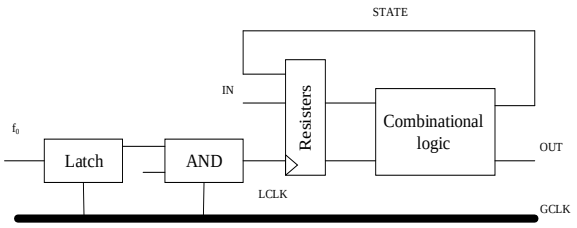

Figure 4 latched clock gating[3]

Principle of clock gating

The clock network in a microprocessor feeds the clock to sequential elements like flip-flops and latches, and to dynamic logic gates[1][2][8].

At a high level, gating the clock to a latch or a logic gate by ANDing the clock with a control signal prevents the unnecessary charging/discharging of the capacitances when the circuit is idle, and saves the circuit's clock power[2][10]. Figure (a) shows the schematic of a latch element.

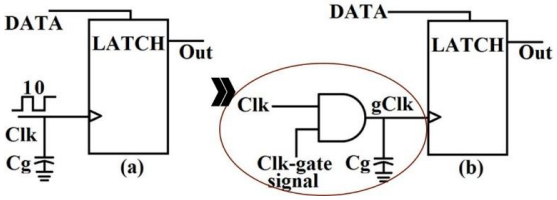

Figure 5 clock gating technique[1]

C_g is the latch's cumulative gate capacitance connected to the clock. Due to clock switches every cycle, C_g performs charging and discharging operation in every cycle and consumes the significant amount of power. The latch still consumes clock power, even if the inputs do not change from one clock ti next.

In figure (b), the clock is gated by ANDing it with a control signal, which we refer as ***Clk-gate signal***[1]. When the latch is not required to switch state, Clk-gate signal is turned off and the clock is not allowed to charge/discharge C, saving clock power. Because the latches of an operand can be driven by an AND gate, the capacitance of the AND gate itself is much smaller than the sum of multiple C_g of these latches. Hence, we can get a net power saving.

Simulations And Results

Simulation start with design of microprocessor. The microprocessor is design using Verilog code. The features of microprocessor

- 100 instructions for operation
- 64K byte memory addressing capacity
- Eight addressing mode
- 16-bit ALU with bit, byte and BCD operations
- Fully synchronous design
- Uniform two clock cycle

Next step of simulation is verification and measurement of power dissipation. This process is done using Altera quartus II. Coding part is done in verilog HDL. Here we mainly measure the power dissipation of microprocessor in normal mode and in clock gated mode. For measurement of power dissipation, we used powerplay power analyzer tool, which is part of Altera Quartus II.

The result is shown in below table. Table shows the total power dissipation, dynamic power dissipation, static power dissipation and IO power dissipation. The changes in dynamic power is measurable for microprocessor.

TABLE 1: COMPARISON OF POWER DISSIPATION

Mode	Total power	Dynamic power	Static power	IO power
Normal	87.80mW	0.10mW	81.35mW	6.35mW
Clock Gating	87.69mW	0.02mW	81.35mW	6.32mW

CONCLUSION

In this paper, microprocessor is design using Verilog HDL in Altera Quartus II tool. Clock gating is applied a datapath using Verilog. The microprocessor which is operated in normal mode, dynamic power dissipation is 0.10mW. When Clock Gating (CG) is applied power is reduced by 0.02mW. Total dynamic power is reduced by 20%.

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