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RESEARCH ARTICLE

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A 0.18µM CMOS HIGHLY LINEAR RF DOWN CONVERSION MIXER FOR 2.4GHZ APPLICATIONS

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ABSTRACT

A highly linear down conversion mixer with moderate gain used for 2.4GHz RF applications is presented in this paper using 0.18µm CMOS technology. The proposed mixer incorporates current bleeding technique & degenerative resistors to improve linearity and conversion gain. Also the negative feedback configuration of the circuit gives flat conversion gain increasing the overall bandwidth. The simulation results reveal that the proposed mixer shows input referred third order input intercept point (IIP3) at 13.13dBm, 1dB compression point at -9.94dBm with conversion gain of 9dB. The circuits operates at 1.8V power supply and dissipates 9mW power.

Keywords—Conversion gain, Gilbert Cell, IIP3, Linearity, Mixer, RF CMOS.

INTRODUCTION

Since last few years, wireless communication has remained in the peak demand. Increasing demand makes engineer to design low power and low cost transceivers [3]. Recently lots of applications has been evolved in unlicensed ISM bands that is free for industrial, scientific, and medical applications. Various protocols, like Bluetooth, IEEE802.11b, IEEE 802.11g and 802.16 standards, have been developed till date in ISM band [7]. All of the above protocols are implemented in same frequency band makingsystems noisy and susceptible to interference. Here comes the role of RF design engineer to make robust designs. Simplified block diagram of RF front end can be shown as below [2]:

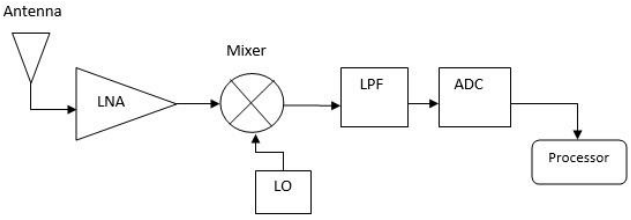

Fig. 1. Front end of the receiver

In RF transceiver, mixer plays an important role to convert either RF signal to intermediate frequency (IF) signal called down-conversion or IF to RF signal called up-conversion [1]. For down conversion IF can be given as

$$\omega_{IF} = \omega_{LO} - \omega_{RF} \quad (1)$$

Thus, mixer is a frequency dependent component that can suffer from interference a lot. So IIP3 of a mixer is a key parameter form which one can decide linearity of the circuit. The spurious free dynamic range (SFDR) denotes the maximum level of

interference that a mixer can tolerate. It can be calculated as below:

$$SFDR = \frac{2}{3}(IIP3 - F) - SNR_{min} \quad (2)$$

Where F represents noise figure, SNR_{min} represents minimum signal-to-noise ratio, and IIP3 is input intercept third order point. From above equation, it can be noted that to improve SFDR, higher IIP3 is required.

There are various techniques prevailing to improve the linearity of mixer. Out of available active mixers design, Gilbert cell is most widely used. In that also double balanced mixer is famous as it can suppress leakage signals at output [1], shown in Figure: 2

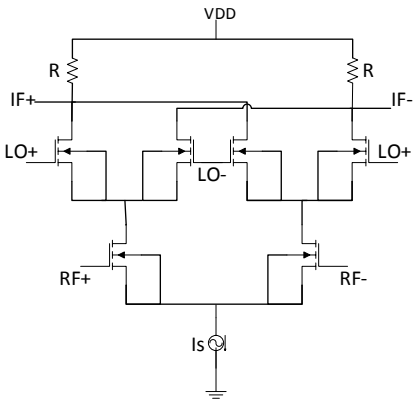

Fig. 2. Double Balanced Gilbert Cell

Non-linearity in circuits causes the power gain to deviate from its ideal value. The point at which the curve is 1dB below the ideal curve is called 1dB compression point (P_{1dB}). The dynamic range of the mixer can be defined from thisP_{1dB} and IIP3 point.The IIP3 of the CMOS Gilbert mixer [8] is approximately given as

$$IIP3 = \sqrt{\frac{32\ Is}{3\ \beta n}} \quad (3)$$

Where Is is the bias current flowing in the input MOSFET.

Design Methodology

Any electronic circuit that make use of active devices always suffer nonlinear phenomenon. For a given NMOS the relationship between the input gate to source voltage and the output drain current is given by

$$I_{OUT} = V_{DC} + gm\ V_{GS} + \frac{gm' V_{GS}}{2!} Vgs^2 + \frac{gm'' V_{GS}}{3!} Vgs^3 + .. \quad (4)$$

Ideally for square law mosfetgm''should be 0. As it has quadratic behavior, current to voltage relation is quadratic hence can be considered as no gm'' term at all. For pseudodifferential pair, IIP3 is infinite. Biasing the differential pair with a current source mosfet, IIP3 will no more be infinite and it will have third order terms. Because output current to input voltage is not only decided by device characteristics but it depends on the input voltage (differential) that will have third order terms unless matching is done either sides. Linearity becomes worse with this increment of gm''[4]. Moreover Biasing point can be increased to increase the linearity but then DC current and the power dissipation increases. For LO stage square wave is given as input to reduce the even order intermodulation products at the output [6]. The Fourier series expansion of the Signum function is given by

$$s(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos(n\omega_{LO})t + b_n \sin(n\omega_{LO})t)\ ] \quad (5)$$

where a_0 and a_n becomes 0 as it's a symmetrical odd square wave. The advantage ofNegative feedback is that it actually opposes the input from its output. Hence reduces the nonlinear interference, improving linearity while talking about active devices. The Principle of linearity states that conversion gain should be independent of the input stage. The source degenerative resistors of 50 ohm are added in the driver stage to increase the linearity at the cost of conversion gain [10]. Neglecting body effects, the transconductance becomes

$$G_m = \frac{g_m}{1+g_m R} \quad (6)$$

Where R is the degeneration resistor. The equation for large $g_m R$ approaches $\frac{1}{R}$ an input independent value. Moreover three current sources are used in the circuit. The lower most provides the bias current and the other two (M_9 and M_{10}) used to implement the current reuse bleeding method to improve the driver current of the trans conductance stage. Current bleeding allows the control of the DC currents for the LO transistors (M_1 to M_4) separately to that of trans conductance stage [8]. In Fig. the effective DC current of the driver stages is the sum of current from the LO stage FET and from the Pmos added [5]. Two LO stage transistors can work as a

single transistor at a time. Therefore, for a given supply voltage, driver current is

$$I_{D(LO)} < I_{D(LO)} + I_{pmos}. \quad (7)$$

Generally for radio frequency integrated circuits the input voltage is kept between 0.3V to 0.6V for the correct operation of the transistor.

$$V_{GS} - V_{TH} \geq V_{safety} \quad (8)$$

Where $300mV \leq V_{GS} \leq 600mV$

In calculating the width of the transistors in was assumed that V_{th} = 0.35v_0.40v and I_s = 1.8mA.

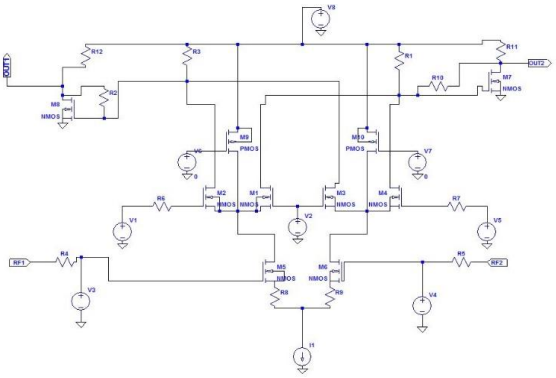

Fig. 3. Proposed Mixer

The double balanced gilbert type mixer topology as shown in figure 2 is taken as a fundamental block since it has many advantages over other topologies. The proposed mixer is divided into three stages. The RF stage, also called transconductance stage is the input stage which receives the RF signal that has to be down converted [10]. It consist of degenerative resistors to improve linearity. The RF voltage is multiplied with the LO signal that is a switching signal at LO stage. Last is the load stage which converts the multiplied current signal into voltage, as shown it is with feedback configuration. Bleeding technique used in the LO stage to reduce the current through switching transistors, improving the $\frac{1}{f}$ noise and gain.

Conversion gain for the proposed structure is given by

$$\text{Conversion Gain} = \frac{4}{\pi} g_m R_L \quad (9)$$

Where g_m is the transconductance of the driver stage transistor and R_L is the load resistance of the circuit which can be calculated using small signal model analysis.

Simulation Results

All simulations were done using Mentor Graphics's Pyxis Schematic, HspiceRF and LTspice Design tool. A RF signal of 2.4GHz is multiplied with the LO signal of 2.5GHz producing the desired down converted intermediate frequency of 100MHz and undesired up-converted frequency of 4.9GHz. The amplitude of LO is taken to be 1.8V for better switching.

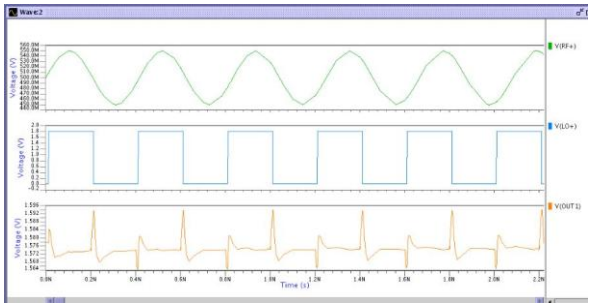

Fig. 4. Input output waveforms

Periodic steady state analysis in mentor graphics tool and harmonic balance simulations in HspiceRF performs the large signal analysis to compute the IIP3 point and 1dB Compression point of the circuit. To find 1dB compression point input power is swept from -50dBm to 20dBm. 1dB compression point is obtained at -9.94dBm.

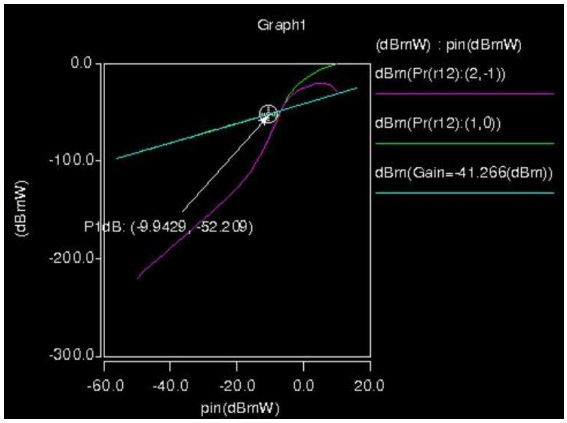

Fig. 5. 1dB Compression Point

To find the IIP3 point, two closely spaced signals (2.4GHz and 2.41GHz) are given as an input and the input power is swept between -50dBm to 20dBm [9]. The two signals will mix with the LO to produce the second order intermodulation (IM2) effects at 100MHz and 90MHz and third order intermodulation effects (IM3) at 1100MHz and 80MHz. The simulation gives IIP3 point at 13.13dBm.

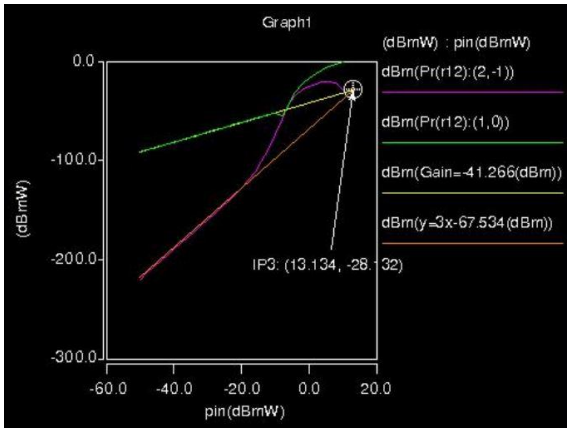

Fig. 6. IIP3 Point

Table 1gives the summary of all simulated results using TSMC 0.18µm CMOS technology.

TABLE 1MIXER PERFORMANCE SUMMARY

Performance Measure	Simulated Results
Power Supply	1.8V
Conversion Gain	9dB
IIP3	13.13dBm
1dB Compression Point	-9.94dBm
Drain Current	1.30mA
Power dissipation	9mW

Conclusions

A highly linear RF down conversion mixer with accepted conversion gain was presented in this paper. Design optimization techniques like degeneration resistors and current reuse bleeding technique were incorporated to improve the performance of the circuit. Negative feedback configuration was chosen to reduce the distortions increasing the overall bandwidth. The design was focused to achieve broad band performance while improving the linearity and gain as was the case in [4] and [6] gilbert-cell designs. The proposed structure was simulated using TSMC 0.18µm CMOS technology in HspicerRF. Use of other designing tool such as MentorGraphics and LTspice was done as well whenever required. The simulation shows third order input intercept point (IIP3) at 13.13dBm dissipating 9mW from 1.8V power supply.

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