International Journal of Engineering Research-Online
A Peer Reviewed International Journal
Articles available online http://www.ijoer.in

Vol.3., Issue.5., 2015
(Sept.-Oct.)

RESEARCH ARTICLE

ISSN: 2321-7758

MULTI-LEVEL INVERTER TOPOLOGY FOR RENEWABLE POWER GENERATION SYSTEM

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ABSTRACT

Multilevel inverters have got high quality output when compared with two-level inverters. so for high power purposes the usage of Multi-level inverter applications has grown more common in industries. In this paper foremost a new topology is developed for the inter connection of renewable energy power generation to grid. With the proposed topology quality of output voltage is improved along with low switching losses. In this topology, the number of switches used for the dc to ac conversion is reduced. So the cost of dc to ac conversion system significantly reduces. The switching technique employed in the converter exhibits some attractive features which suits industrial applications. Analysis and realization of the circuit topology is carried out in MATLAB Simulink environment.

KEYWORDS: Multilevel inverter, quality output, solar energy, MATLABSIMULINK software.

I. INTRODUCTION

Nowadays, for high power and high voltage applications, multi-level inverters are used because of their advantages like its output voltage has got lower electromagnetic interference, reduced harmonic distortion, high efficiency. Multi-level inverters includes power semiconductors devices and dc voltage sources, the output is generated with voltages of stepped waveform. In Multi-level inverters, required ac output voltage waveform can be obtained by various combinations of multiple dc voltage sources. As the number of voltage sources increased, the quality of output voltage is much improved. [1]. However, a larger number of levels increase the number of devices that must be controlled. The attractive features of multi-level inverter are that they can generated the output voltages with very low THD, can draw input current with low distortion, and can operate at wide range of frequencies from fundamental frequency to very high frequency.

There are three well-known types of Multi-level inverters, the neutral point clamped (NPC) or diode clamped multilevel inverter [2], the flying capacitor (FC) multilevel inverter [3], and the cascaded H-bridge (CHB) multilevel inverter[4]. All these three conventional single phase inverters, for three levels output are shown in Fig(1). The NPC Multi-level inverter has got the drawback of the unequal voltage distribution between the series

connected capacitors, which causes the dc-link capacitor unbalancing and require large number of clamping diodes for a large number of voltage levels. The FC multilevel inverter uses flying capacitors as the clamping devices and this type topology has got several advantages when compared to NPC Multilevel Inverters, also with the advantage of having redundant phase leg states which allows the equal distribution of switching stress among the semiconductor devices and also the transformer less operation. The output voltage of conventional multi-level inverter is as shown in fig (2).

The topologies of cascaded h-bridge multi level inverter [6]have got good modularity and simplicity of control and so they are suitable for high-voltage applications. But, the drawback of this topology is it requires large number of separated voltage sources to supply each conversion cell, [5].To overcome this drawback for high voltage applications, new configurations have been developed. These multi-level inverters also got some particular disadvantages like, they require large number of power semiconductor devices, which leads to increase in the cost and complexity in controlling and tend to reduce the efficiency and overall reliability.

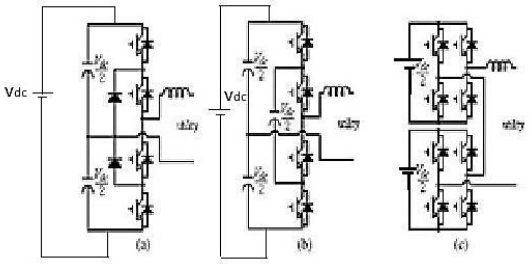


Fig (1).(a) Diode Clamped Multilevel Inverter
(b) Capacitor Clamped Multilevel Inverter
(c) Cascaded H–Bridge Multilevel Inverter.

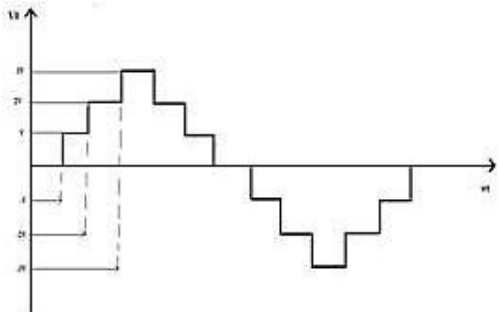


Fig (2): Output voltage of conventional seven-level multi level inverter

In the conventional inverters single dc source is employed but in the proposed topology series connection of two dc sources with different ratings are used. Among all these multi level inverters, the proposedtopologies got many advantages and are preferred mostly. In the past years, lot of configurations and topologies are presented in order to reduce the total number of devices. Some among them are proposed in the literature.

II.RENEWABLE ENERGY:

Renewable energy sources are also called as non-conventional type of energy, which are continuously replaced by natural process Such as solar energy, wind energy, hydropower, and bio-energy etc., are some of examples of renewable energy sources. A renewable energy system convert the energy found in sunlight, falling-water, wind, sea-waves, geothermal heat, or biomass into a form, which we can use in the form of heat or electricity. The majority of the renewable energy comes either directly or indirectly from sun and wind and can never be exhaustion, and therefore they are called renewable.

However, the majority of the world's energy sources came from conventional sources-fossil fuels such as coal, natural gases and oil. These fuels are often term non-renewable energy sources. Though, the available amount of these fuels are extremely large, but due to decrease in level of fossil fuel and oil level day by day after a few years it will end [7]. Hence renewable energy source demand increases as it is environmental friendly and pollution free which reduces the greenhouse effect.

A. Solar energy:

Solar energy is a rapidly available non-conventional type of energy. The energy from the sun is in the form of irradiation. Solar energy has been hamessed by humans since ancient times using a variety of technologies.

Solar powered electrical generation relies on photovoltaic system and heat engines. Solar energy's uses are limited only by human creativity. To harvest the solar energy, the most common way is to use photo voltaic panels which will receive photon energy from sun and convert to electrical energy.

B. Photovoltaic cell:

A photovoltaic cell or photoelectric cell is a semiconductor device like silicon which coverts light energy into electric energy by photovoltaic effect. For solar cells, a thin wafer consisting of a very thin layer of phosphorous- doped(N-type) silicon on top of thick layer of boron-doped(P-type) silicon. When light energy strikes the solar cell, electrons are knocked loose from the atom in semiconductor material [8]. A PV cell can either in circular or in square construction. The equivalent circuit of solar cell is as shown in fig (4).

C. Photovoltaic module:

A single solar cell generates a very low voltage (around 0.5V) so more than one PV cell is connected in series or parallel to form a module for desired output. Series connections are responsible to increase a voltage of the module whereas parallel connections are responsible to increase a current of the module[9]. Separate diodes may be needed to avoid reverse currents.

D. Photovoltaic array:

The power that one module can produce is not sufficient to meet the requirements of home or business. Most PV arrays use an inverter to convert the DC power into alternating current that can power the motors, loads, lights etc. The modules in a PV array are usually first connected in series to obtain the desired voltages, the individual modules are then connected in parallel to allow the system to produce more current. The arrangement of photovoltaic array system is as shown in fig (3).

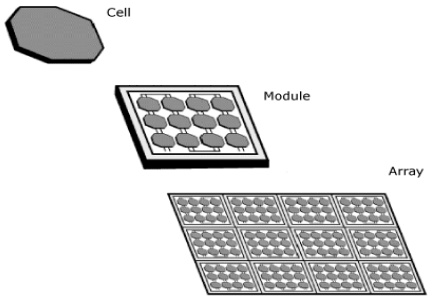


Fig (3): photovoltaic system

E. Modeling of pv array:

The current source Iph represents the cell photo current, Rsh and Rs are used to represent the intrinsic series and shunt resistance of the cell respectively. Usually the value of Rsh is very large and that of Rs is very small, hence they may be neglected to simplify the analysis. PV cells are grouped in larger units called PV modules which are further interconnected in series-parallel configuration to form PV arrays [10], [11].and the equivalent circuit of single solar cell is as shown in fig (4).

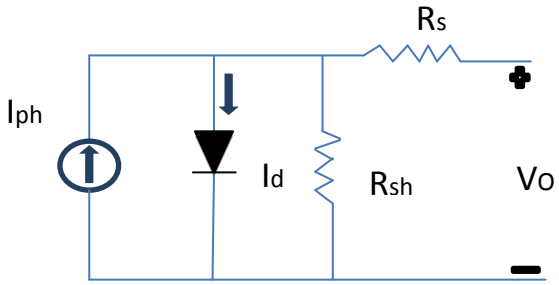


Fig (4): equivalent circuit of solar cell

The PV mathematical model used to simplify our PV array is represented by the equation: $I = I_{PH} - I_S \left[exp\left(\frac{q(V+IR_S)}{kT_CA}\right) - 1\right] - (v + IR_s)/R_{SH}$..... *(1)*

Where,

I is the PV array output current;

V is the PV array output voltage;

Ns are the number of cells in series and Np is the number of cells in parallel;

q is the charge of an electron;

k is the Boltzmann's constant;

A is the p-n junction ideality factor;

T is the cell temperature (K);

I_{RS} is the cell reverse saturation current.

The factor A in equation (1) determines the cell deviation from the ideal p-n junction characteristics; A is dependent on PV technology.

The photo current I_{PH} depends on the solar radiation and cell temperature as follows

$I_{PH} = \left[I_{scr} + k_i\left(T_c - T_{Ref}\right)\right]\lambda$..... (2)

Where

I_{scr} is the cells short-circuit current at reference temperature and radiation, K_i is the short circuit current temperature coefficient, and S is the solar radiation in KW/m2.

The approximate model PV solar cell with suitable complexity so equation (1) can be written as

$I = I_{PH} - I_S \left[exp\left(\frac{q(V+IR_S)}{KT_CA}\right) - 1\right]$..... .*(3)*

After neglecting R_S& R_{SH} .The above equation can be written as:

$I=I_{PH}-I_S\left[exp\left(\frac{q(V)}{KT_cA}\right)-1\right]$..... *(4)*

The cell saturation current I_{RS} varies with temperature according to the following equation

$I_S=I_{RS}(T_C/T_{Ref})^3 exp\left[qE_G\left(\frac{1}{T_{Ref}}-\frac{1}{T_C}\right)/kA\right]$... *(5)*

Where,

T_{REF} is the cell reference temperature,

I_{RS} is the cell reverse saturation temperature at T_r

E_G is the band gap of the semiconductor used in the cell.

The reverse saturation current at reference temperature can be approximately obtained as

$I_{RS}=I_{sc}\ /[\exp\left(\frac{qV_{OC}}{kAT_C}\right)-1]$..... *(6)*

The PV power can be calculated using equation as follows:

$P=V_{max}I_{max}$..... (7)

Where V_{max} and I_{max} are terminal voltage and output current of PV module.

The current to voltage characteristic of a solar array I-V and P-V curve for fixed level of solar irradiation and temperature are shown.

III. PROPOSED TOPOLOGY:

1. seven-level topology:

The circuit shown in Fig (7) is a seven – level inverter comprising of two DC voltage sources (capacitors acts as sources) V1 and V2, six switches and two diodes (S1, S2, D2, D3, T1, T2, T3 and T4). Thetwo switches (S1, S2) generate a step outputfrom two sources which is similar to the output obtained from a full wave rectifier as shown in fig (5).

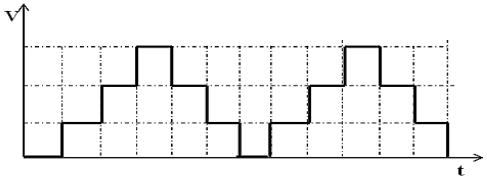


Fig (5): step output

And then the remaining four switches (T1, T2, T3 and T4) are used as H-Bridge inverter which converts positive half cycle of output to negative representing a sine wave is as shown in fig (6).

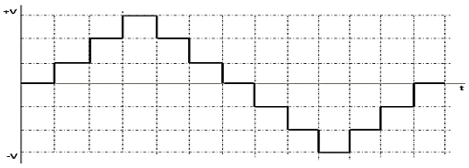


Fig (6): seven level output

At the output terminals ofH-Bridge inverter the load is connected. Therefore, by using H-Bridge inverter at the end, the entire generated positive half – cycles will be converted into positive and negative half – cycles.

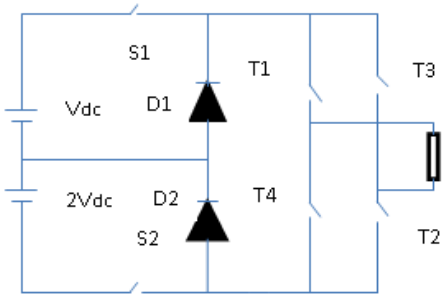


Fig (7): Seven – Level Proposed Topology

A. Principle of operation:

The operation of this seven-level inverter can be divided into eight modes. Modes 1-4 are for the positive half cycle, and modes 5-8 are for the negative half cycle. Fig 8 shows the operation modes of seven-level inverter. Fig 8(a)-(d) the power electronic switches T1 and T2 are in the ON state. And the power electronic switches T3 and T4 are in OFF state during the positive half cycle. On the contrary the power electronics switches T1 and T2 are in OFF state and the power electronics switches T3 and T4 are in ON state during the negative half cycle. Since the DC capacitor voltages Vc1 and Vc2 are balanced by controlling the seven-level inverter. The dc capacitor voltages Vc1 and Vc2 can be expressed as follows:

Vc1=Vdc, Vc2=2Vdc

The switching modes and output voltages of seven level multilevel inverter as shown in table(1).

The modes of operation for seven-level inverter are as follows:

Mode-1: fig.8(a) Shows the operation circuit of mode-1. In this mode the power electronic switch S1 is turned ON and S2 is turned OFF. DC capacitor C1 is discharged through switches S1→T1→load→T2→D3, and forms the loop. The output during this mode of operation is Vdc.

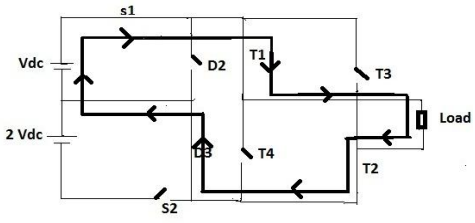
Mode-2: fig.8 (b) shows the operation circuit of mode-2. In this mode the power electronic switches S2 is turned ON and S1 is turned OFF. Dc capacitor C2 is discharged through switches D2→T1→load→T2→S2, and forms the loop. The output during this mode of operation is 2Vdc.

Mode-3: fig.8(c) shows the operation circuit of mode-3. In this mode the power electronic switches S1 and S2 both are turned ON. Dc capacitors both are discharged together through switches S1→T1→load→T2→S2, and form the loop. The output during this mode of operation is 3Vdc.

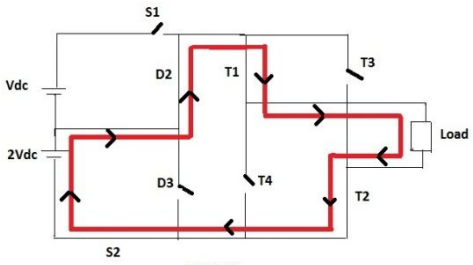
Mode-4: fig. 8(d) shows the operation circuit of mode-4.In this modeboth power electronic switches S1 and S2 are turned OFF.The current flows through the switches T1→load→T2→D3→D1, and forms the loop. The output during this mode of operation id zero.

Similarly the principles of working of modes 5-8 are similar to modes 4,3,2, and 1 respectively. But the modes from 5-8 are for negative half-cycles, so switches T1 and T2 are turned OFF and switches T3 and T4 are turned ON. The output voltage obtained from modes 5-8 are 0, -Vdc, -2Vdc and -3Vdc respectively. Therefore, the generated outputs of proposed topology are as follows +3Vdc, +2Vdc, +Vdc, 0, -Vdc, -2Vdc, and -3Vdc.

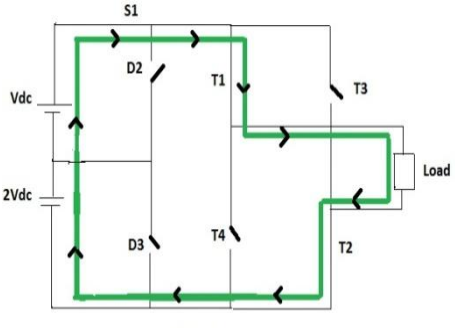
B. Modes of operation of 7-level multi level inverter:



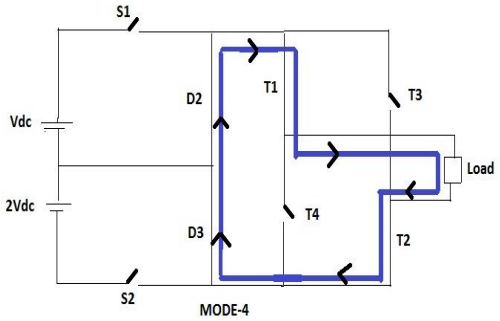
Mode-1



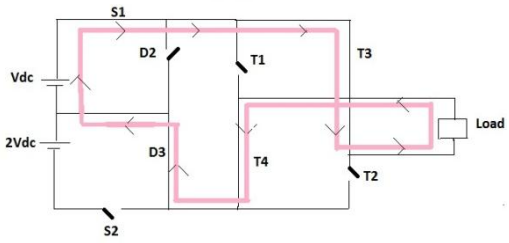
MODE-2



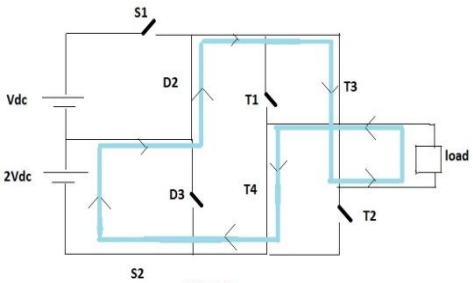
MODE-3



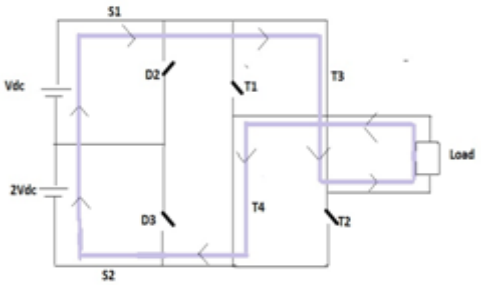
MODE-4



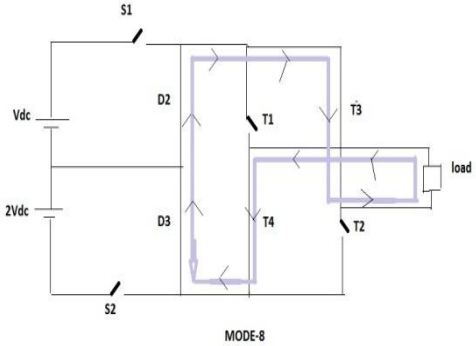
MODE-5



MODE-6



Mode - 7



MODE-8

Fig(8): Modes of operations of seven-level inverter

Table (1) switching table of seven-level inverter

Mode	S1	S2	T1T2	T3T4	V0
1	ON	OFF	ON	OFF	+Vdc
2	OFF	ON	ON	OFF	+2VDC
3	ON	ON	ON	OFF	+3Vdc
4	OFF	OFF	ON	OFF	0
5	ON	OFF	OFF	ON	-Vdc
6	OFF	ON	OFF	ON	-2Vdc
7	ON	ON	OFF	ON	-3Vdc
8	OFF	OFF	OFF	ON	0

2. 31-level proposed topology:

The circuit configuration for the 31-level inverter is as shown in fig (9). For generating a 31-level, 4 constant dc voltage sources (V1=Vdc, V2= 2Vdc , V3=4Vdc , V4=8Vdc) and 8switching devices (S1,S2,S3,S4, T1,T2,T3,T4) are required. Switches S1-S4 acts as sub-multi level inverter, and positive half cycleof this output voltage fed to switches T1-T4 which form a H-bridge inverter and it changes the polarity of the positive half cycle into positive and negative half cycles generating the required 31-level output voltage.

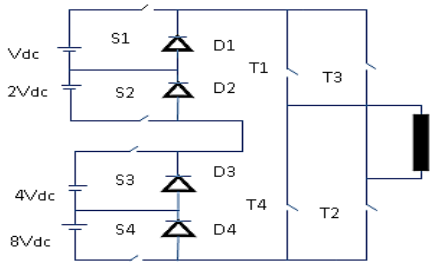
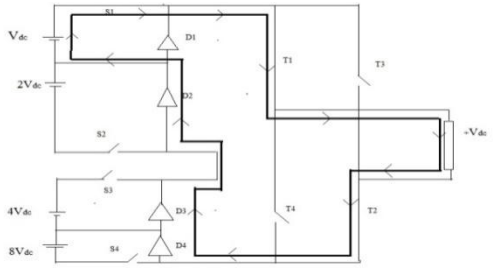


Fig (9) 31-level proposed topology

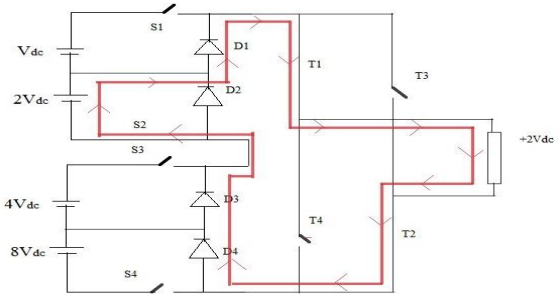
As compared with cascaded multi level inverter, the number of switches used in 31-level proposed topology is less. In cascade multi level inverter for generating 31-level output 4 voltage sources and 15 switches are required [12]. But in this proposed topology for generating 31-level output 4 voltage sources and only 8 switches are required. So switching losses will be reduced, THD will be reduced and also the cost will be reduced. In cascade multi level inverter two types of switches are used for operating low (MOSFET) and high (IGBT) voltage rating but in this topology only one type of switches (IGBT) are used. The switching operation for 31-level inverter is as shown in table (2).

The switching operation for mode 17-31 is similar to that of modes 1-16 except the switches T1T2 will be OFF and switches T3T4 will be ON for negative half cycle. In 7-level multi-level inverter two dc sources and 6 switches are used and by cascading another similar 7-level inverter it acts as a 31-level inverter. Finally 4 voltage sources and 8 switches are required for generating the 31-level output. The working principle is same and conduction of switches is different for different levels.

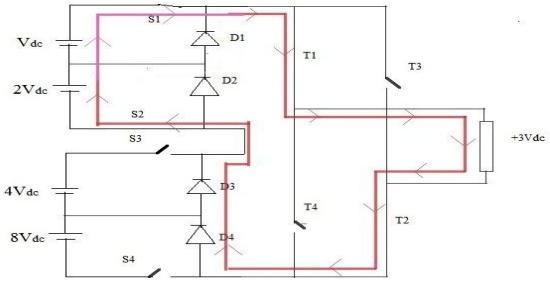
A. Modes of operation of 31-level multi level inverter:



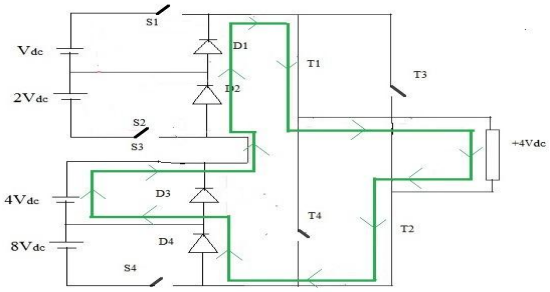
(a) Mode-1



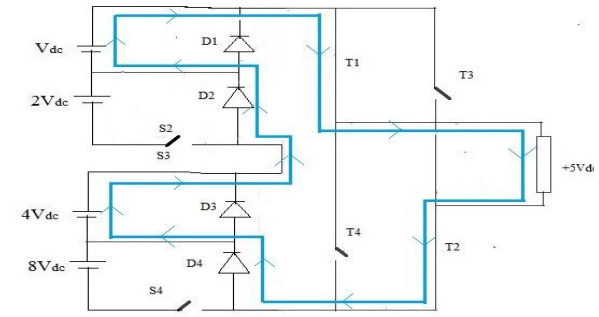
(b) Mode-2



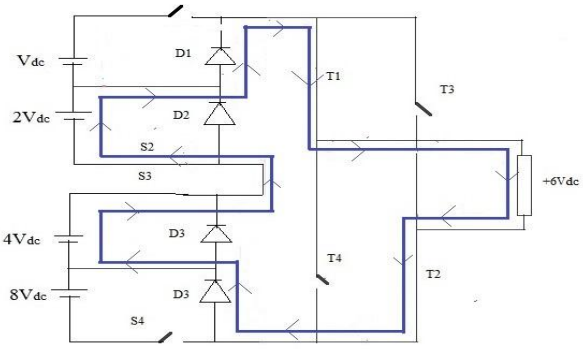
(c) Mode-3



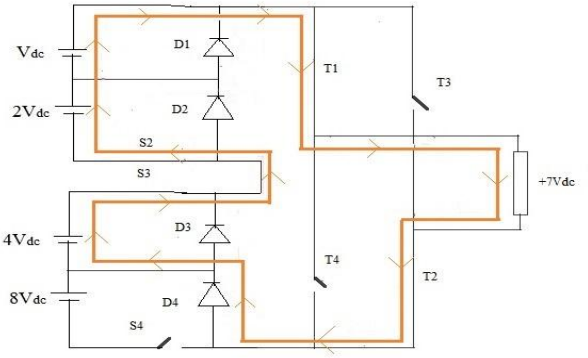
(d) Mode-4



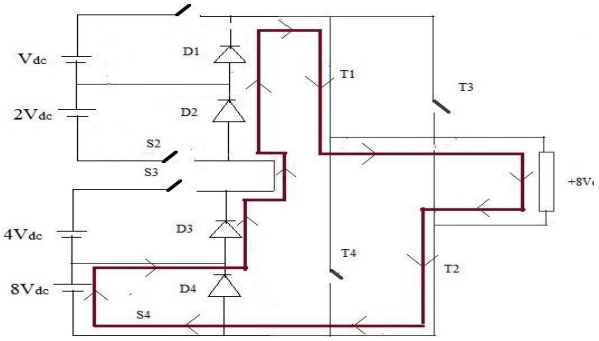
(e) Mode-5



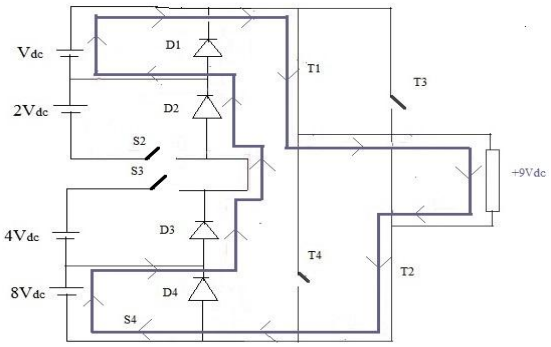
(f) Mode-6



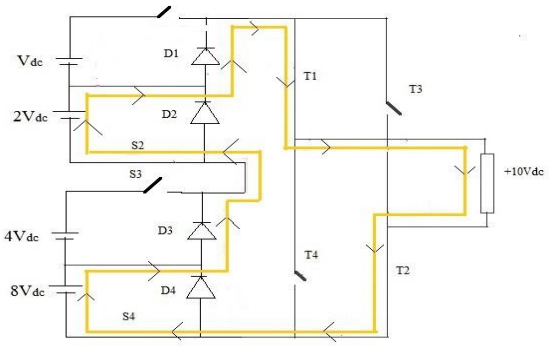
(g) Mode-7



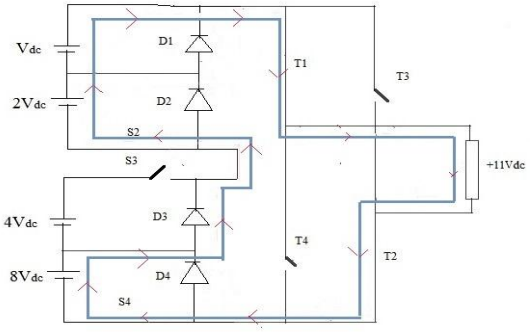
(h) Mode-8



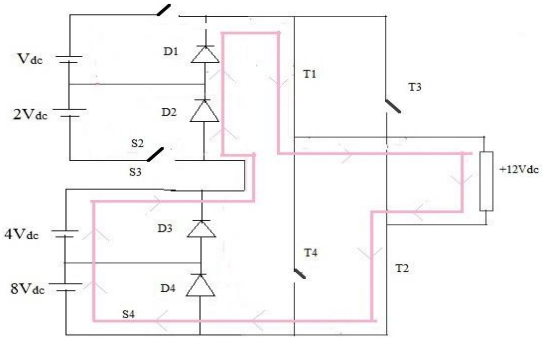
(i) Mode-9



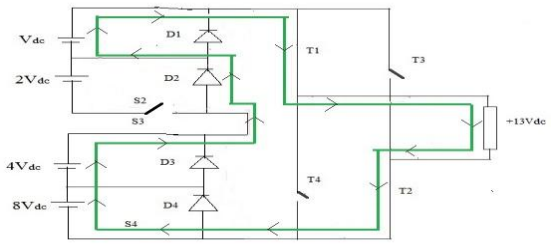
(j) Mode-10



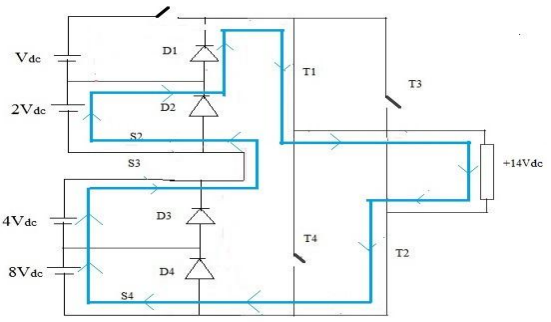
(k) Mode-11



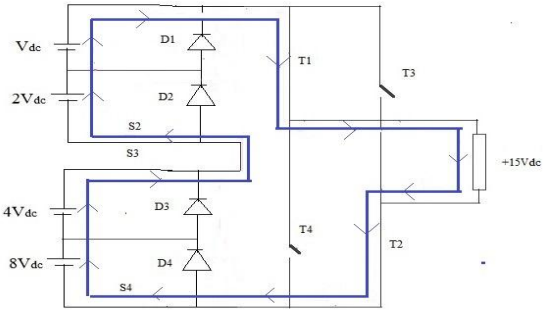
(l) Mode-12



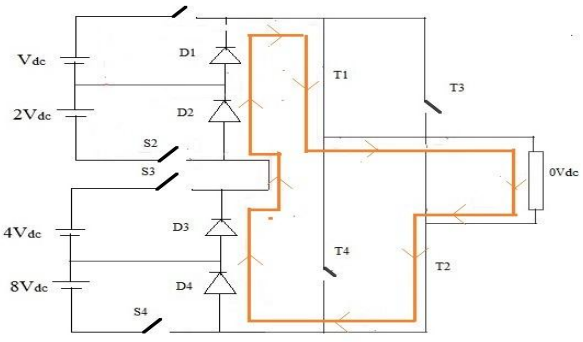
(m) Mode-13



(n) Mode-14



(o) Mode-15



(p) Mode-16

Fig (10): Modes of operation of 31-level multi level inverter for positive half cycle

S.NO	SWITCHES						OUTPUT VOLTAGE
	S1	S2	S3	S4	T1T2	T3T44	
1	ON	OFF	OFF	OFF	ON	OFF	+Vdc
2	OFF	ON	OFF	OFF	ON	OFF	+2Vdc
3	ON	ON	OFF	OFF	ON	OFF	+3Vdc
4	OFF	OFF	OFF	ON	ON	OFF	+4Vdc
5	ON	OFF	ON	OFF	ON	OFF	+5Vdc
6	OFF	ON	ON	OFF	ON	OFF	+6Vdc
7	ON	ON	ON	OFF	ON	OFF	+7Vdc
8	OFF	OFF	OFF	ON	ON	OFF	+8Vdc
9	ON	OFF	OFF	ON	ON	OFF	+9Vdc
10	OFF	ON	OFF	ON	ON	OFF	+10Vdc
11	ON	ON	OFF	ON	ON	OFF	+11Vdc
12	OFF	OFF	ON	ON	ON	OFF	+12Vdc
13	ON	OFF	ON	ON	ON	OFF	+13Vdc
14	OFF	ON	ON	ON	ON	OFF	+14Vdc
15	ON	ON	ON	ON	ON	OFF	+15Vdc
16	OFF	OFF	OFF	OFF	OFF	OFF	0Vdc
17	ON	OFF	OFF	OFF	OFF	ON	-Vdc
18	OFF	ON	OFF	OFF	OFF	ON	-2Vdc
19	ON	ON	OFF	OFF	OFF	ON	-3Vdc
20	OFF	OFF	ON	OFF	OFF	ON	-4Vdc
21	ON	OFF	ON	OFF	OFF	ON	-5Vdc
22	OFF	ON	ON	OFF	OFF	ON	-6Vdc
23	ON	ON	ON	OFF	OFF	ON	-7Vdc
24	OFF	OFF	OFF	ON	OFF	ON	-8Vdc
25	ON	OFF	OFF	ON	OFF	ON	-9Vdc
26	OFF	ON	OFF	ON	OFF	ON	-10Vdc
27	ON	ON	OFF	ON	OFF	ON	-11Vdc
28	OFF	OFF	ON	ON	OFF	ON	-12Vdc
29	ON	OFF	ON	ON	OFF	ON	-13Vdc
30	OFF	ON	ON	ON	OFF	ON	-14Vdc
31	ON	ON	ON	ON	OFF	ON	-15Vdc

Table (2): switching table of 31-level inverter

IV. Simulation results & Discussion:

MATLAB SIMULINK based simulation tool is used to verify the results of i-v and p-v characteristics of PV panel and proposed topologies. Fig (11) & (12) shows the i-v and p-v characteristics of solar cell at different irradiations, as the radiation increase the voltage, current increases which increase the power. Fig (13) & (14) shows the i-v and p-v characteristics of solar cell at different temperatures respectively, as the temperature increases voltage will be decreased but current remains constant hence power will get decreased.

The seven-level output voltages, THD as shown in figure (15)& (16) andthe 31-level output voltage, THD as shown in fig (17)& (18) which shows that as the level of voltage increases, the THD get decreased.

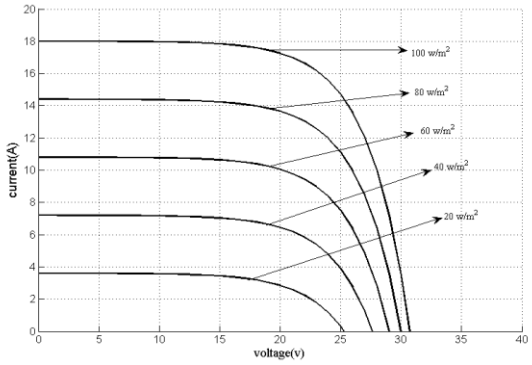


Fig (11): i-v characteristics of solar cell at different radiations

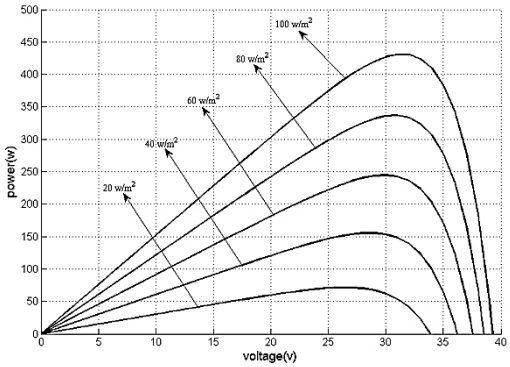


Fig (12): p-v characteristics of solar cell at different radiations

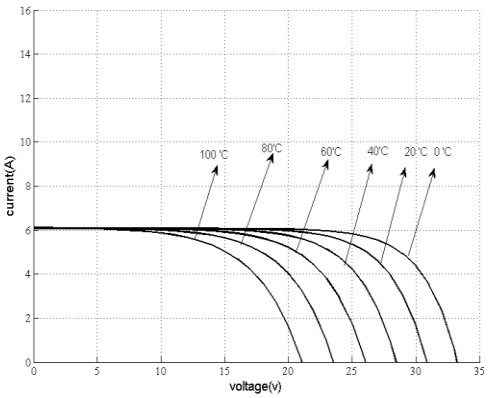


Fig (13): i-v characteristics of solar cell at different temperatures

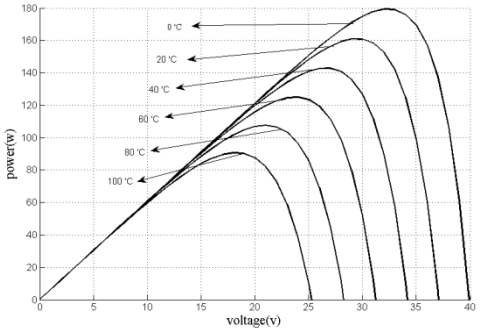


Fig (14): p-v characteristics of solar cell at different temperatures

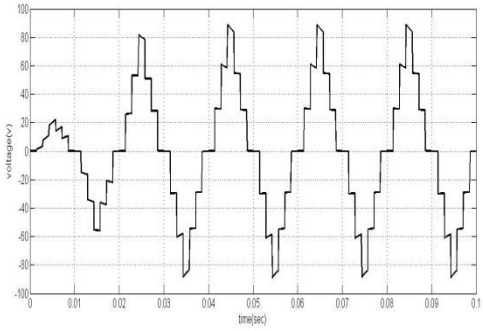


Fig (15): seven level output voltage

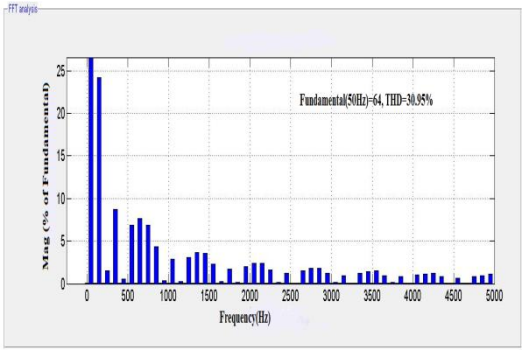


Fig (16) : THD of seven level output voltage

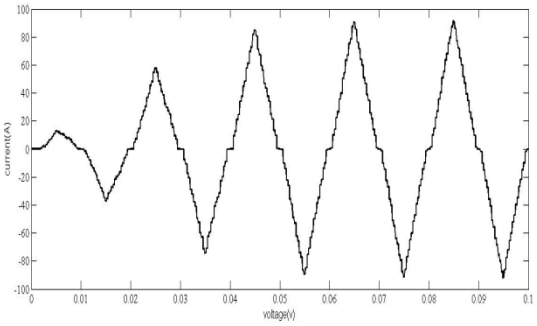


Fig (17): 31-level output voltage

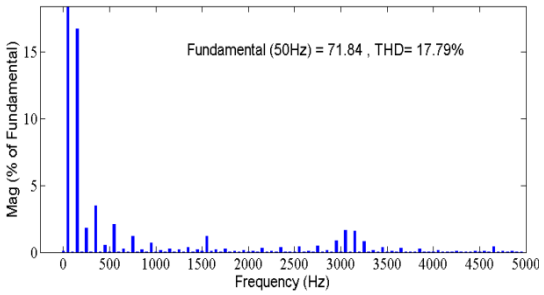


Fig (18) : THD of 31-level output voltage

V. CONCLUSION:

In this paper, a new topology has been introduced for Multi-level inverters. The proposed topology results in reduction of cost and installation area as the number of voltage sources and switches are minimized. This configuration extends possibilities to optimize it for various objectives and the design flexibility. The simulation results for proposed multilevel inverter topology demonstrate that the proposed configuration has prominent feature compared to other conventional Multi-level inverters.

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