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RESEARCH ARTICLE

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GENERIC CONSTRUCTS FOR DESIGN LEVEL TESTING

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ABSTRACT
Verification and design engineers needs a common or single unified verification and design language that allows simulating the HDL design and verified with test bench constructs. This paper focused on generic constructs and designed by using System Verilog HDL as well as two designs (DUT) are verified with single test bench .Test bench includes several constructs that generates different logic. That specifically state what type of logic should be initiated. This singe test bench verify the correction of the Design. Questa Sim 10.0 is used for the simulation purposes.
Keywords: System Verilog, Mil-std 15530, Encoder, Decoder, Test bench

1.0 INTRODUCTION

The method of verification parallels the design creation process. Generic Constructs is the process of verification, proving that designs are functionally corrects or fully tested. Random stimulus inherently ensures the corner case scenarios. Generic constructs in the test bench can be defined in System Verilog HDL. System Verilog provides a very powerful mechanism to generate random stimulus. The SystemVerilog language supports three assistance over Verilog. They are explicit design intent, High level of abstraction, Conciseness of expressions. These benefits improve the test bench portability and readability. The purpose of the test bench is to examine the correctness or functionality of the Design Under Test (DUT).

The main advantage of the test bench is to determine (predestined) the correctness of the design under test (DUT). The figure shows the main operation of the test bench. It generates the stimulus and applies the stimulus to the DUT. After that system capture the response and verify the output response.

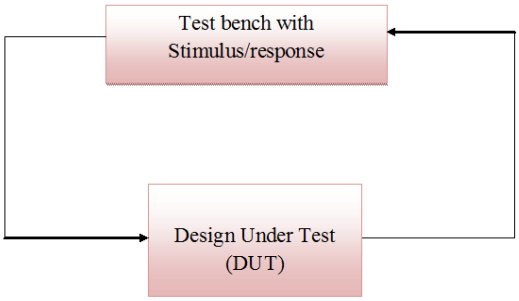

Figure.1 Generic Structure of Test bench

2.0 TEST ENVIRONMENT

The Questa Sim is the advanced simulator, which supports fast time to next simulation and library management. With its unique capability to pre-optimize and design debug visibility are maintain high performance during the verification process. Questa have multi core option which increases the simulation time.

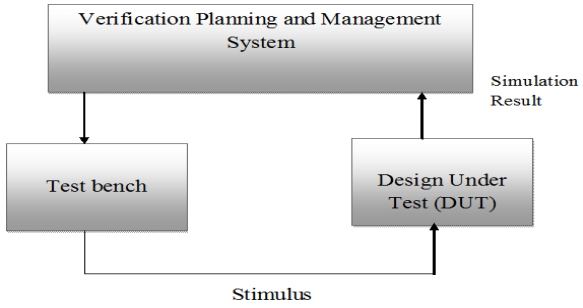

Figure.2 Functional Simulation method

The Questa Sim 10.0 EDA tool is used for the system realization. Design Under test has been characterised in Verilog and Test bench has been characterized in SystemVerilog.

3.0 TEST BENCH DEVELOPMENT STRATEGIES

Test bench developed invoke the functional design and then simulate it. All the test benches are written in SystemVerilog. Test benches are developed to test the design with the following objectives.

- All the functionalities of the IPs are checked including all error conditions.
- To get maximum statement coverage, Branch Coverage, Toggle coverage and FSM Coverage.
- To toggle all the output, input and I/O ports.

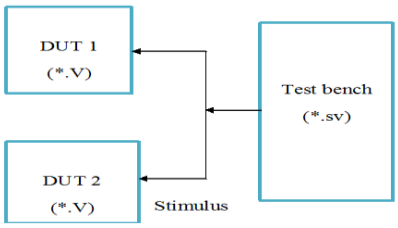

Figure 3.Test bench approach

Figure 3 shows the functional verification of designs using test bench. Multiple designs are verified with single test bench. Interface mechanism provides the connection between the design under test just named as bundle of wires. The interface block provide the additional connection easily, no connections are missed.

Example : MIL –STD Manchester Encoder - Decoder

3.1 Manchester Encoder

To work an encoder, it requires a single clock with a frequency of double the data rate applied at the SEND CLOCK input [1]. The Encoder's cycle starts with ENCODER ENABLE and it is high for one word length or twenty ENCODER SHIFT CLOCK . During the transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input generates command sync or a low will initiate data sync. When the Encoder is acquire to the data, at the same time SEND DATA output will go high for sixteen ENCODER SHIFT CLOCK. When the every high to low transition of ENCODER SHIFT CLOCK, the acquired data should be clocked into the SERIAL DATA input and sampled on the low to- high transition ENCODER SHIFT CLOCK . BIPOLAR ONE and BIPOLAR ZERO are the two Manchester II coded data outputs. The sampled data is send through the BIPOLAR ONE and BIPOLAR ZERO outputs with parity. ENCODER ENABLE must go low to prevent a consecutive word from being encoded. To cut-offs the Encoder transmission ,a positive signal applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

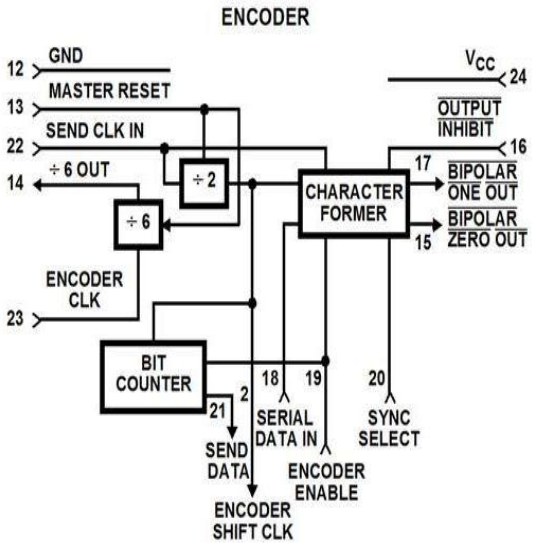

Figure 4. Block Diagram of Encoder

3.2 Manchester Decoder

The Decoder needs a single clock with a frequency of 12 times the required data rate applied at the DECODER CLOCK input. Manchester II encoded data can be transmitted BIPOLAR ONE and BIPOLAR ZERO inputs [1]. The UNIPOLAR DATA input can only acquire the non-inverted Manchester II encoded data. The Decoder is continuously monitors valid sync character . valid sync may be COMMAND/DATA SYNC .If the sync character was command sync, output will go high for sixteen DECODER SHIFT CLOCK ,

otherwise it will produce a data word. The TAKE DATA output will go high and Decoder is sending the decoded data through SERIAL DATA OUT in NRZ. At the same time, all sixteen decoded data bit is checked for odd parity. high on VALID WORD output indicates the successful reception of a word without parity errors.

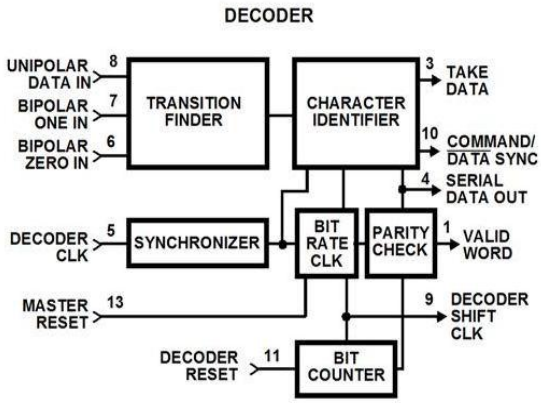

Figure 5. Decoder block diagram

The given figure 6 shows the DUT block of the Manchester Encoder.The test bench signal naming is common and DUTs are different.If clock signal or enble signal in the test bench is represented by ic12 or ee ,where it is different from the clock (clk) or enable (ee_1) of the DUT.The example 1 shows ,How to portmap two different signal using systemVerilog HDL.

DUT _signal (Test bench_signal)
.clk(ic12)
.ee_1(ee)

Example 1. Portmap representation

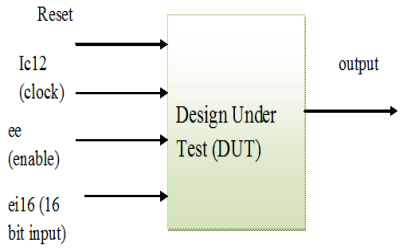

Figure.6 DUT Block

4.0 RESULTS

In this section simulation results are described. The above Manchester encoder and decoder design has been successfully employed. The simulation result proves the performance of the design. MIL STD - 15530 experimental results is shown in figure (7 & 8).

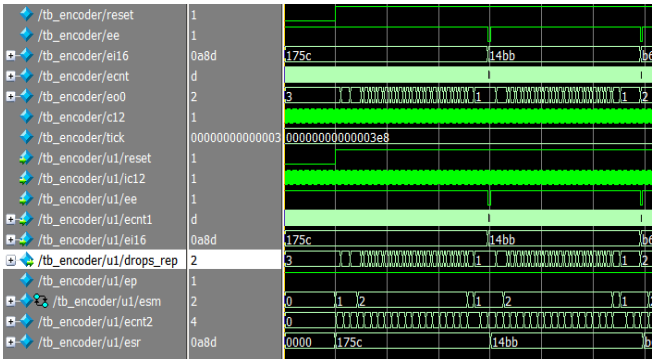

Figure 7. Manchester encoder

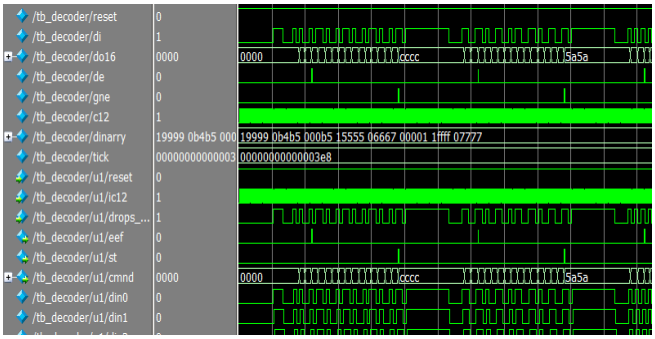

Figure .8 Manchester Decoder

5.0 CONCLUSION

A new method for design level verification using generic constructs has been presented .Which introduces high level verification with SystemVerilog test bench approach. Mil-Std 15530 Manchester Encoder and Decoder is used for this experiment. The functionality of the design is verified with unique test bench. Single test bench has been characterized in SystemVerilog. The simulation results determined the several benefits of the design as shown.

1) The method is reliable and simple.
2) Easy to be implemented
3) Easy to Verified.

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