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RESEARCH ARTICLE

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A NEW INVERTER WITH FEWER SWITCHES FOR REDUCTION OF HARMONICS AND VARIATIONS IN TORQUE FOR SYNCHRONOUS DRIVES

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ABSTRACT
In a regular Brush less DC motor (BLDC) drive, the motor in general fed with Pulse Width-Modulated (PWM) voltages which cause steep voltage wave fronts (*dv/dt*) to materialize across the motor terminals. This may possibly escort the motor insulation stoppage. In addition, motor damages are reported due to the high-voltage change rates (*dv/dt*) which produces common-mode voltages athwart the motor windings. Elevated frequency switching increases the gravity of this drawback due to the increased number of times. In each cycle this common-mode voltage is functional. For variable-speed medium-voltage drives this is a piece of big concern where the voltage levels are incredibly far above the ground. The expected problem can be resolved by applying variable voltage with low *dv/dt* i.e., making the use of multilevel inverter. In this proposed topology, power cells linked in cascade using two inverter legs in series, as an alternative of two parallel inverter legs, set up in CHB power cells, conservatively. In this proposed topology input voltage is Vdc/2 and in condition any module goes amiss, and the topology can maneuver with shortened output voltage and consequently reduced power. So that severity of explosion is reduced to half and results in increase of the reliability of the system and cost effectual. Detailed analyses of the proposed structure with five levels are carried out using pulse width-modulation phase-shifted multicarrier modulation. Finally seven level Cascaded multilevel inverter fed Brushless dc motor drive is implemented in Matlab / Simulink and simulation results are presented for verification and validation of the proposed work.

Key words: Cascaded H-Bridge (CHB) Multilevel inverter (MLI), Total harmonic distortion (THD), Pulse Width Modulation (PWM), Switching frequency.

I. INTRODUCTION

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages [1],[2],[3]. Fig. 1 shows a schematic diagram of one phase leg of inverters

with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor Fig. 1(a), while the three-level inverter generates three voltages, and so on. Most prominent among them are high efficiency and high power density due to the absence of field winding, in addition the absence of brushes leads to high reliability, low maintenance and high capability. However in a practical BLDC drive, significant torque pulsations may arise due to the back emf waveform departing from the ideal. as well as commutation torque ripple, pulse width modulation (PWM) switching. Torque ripple due to the current commutation is caused by the mismatches between the applied electromotive force and the phase currents with the motor electrical dynamics. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion [4], [5].

Nowadays researchers are trying to reduce the torque ripple and harmonic component in the BLDC motor. An active topology to reduce the torque ripple is synchronous motor presented in [1]. This paper discusses the hysteresis voltage control method. The torque ripple is minimized using PWM switching is presented in paper [2], this scheme has been implemented using a PIC microcontroller to generate modified pulse width modulation (PWM) signals for driving power inverter bridge. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: diode-clamped or neutral point clamped, flying capacitors clamped and cascaded multi cell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (SPWM).

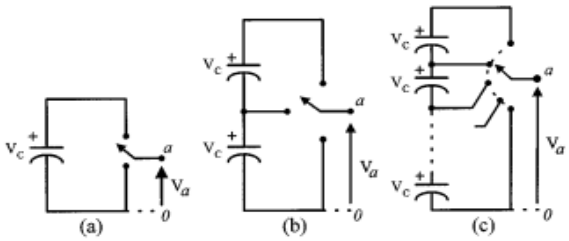

Figure 1. One phase leg of an inverter with (a) two levels, (b) three levels, and (c) N levels

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM) [6],[7],[8].The attractive features of a multilevel converter are, (a) *Staircase waveform quality:* Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.*(b) Common-mode (CM) voltage:* Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. (c) *Input current:* Multilevel converters can draw input current with low distortion. (d) *Switching frequency:* Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. There are different approaches for the selection of switching techniques for the multilevel inverters.

II. FUNCTIONAL UNITS

The BLDC Motor requires a power electronic drive circuit and a commutation system for its operation. The Fig.1 describes the functional units present in the drive circuit and the associated commutation controller for the BLDC Motor. A 4 pole BLDC motor is driven by the inverter for 120 degree commutation. The rotor position can be sensed by a hall-effect sensor, providing three square wave signals with phase shift of 120^0. These signals are decoded by a combinational logic to provide the firing signals for 120^0 conduction on each of the three phases. The operation of the system is as follows: as the motor is of the brushless dc type, the waveforms of the armature currents are

quasi square. These currents are sensed through current sensors, and converted to voltage signals. These signals are then rectified, and a dc component, with the value of the ceiling of the currents, Imax, is obtained as shown in Fig.2 This dc signal is compared with a desired reference Iref, and from this comparison, and error signal Ierr is obtained. This error is then passed through a PI control to generate the PWM as shown in Fig.3 for all the switches of the multi-level inverter which are sequentially activated by the shaft position sensor.

Fig.2 Current Controller of BLDC Motor with MLI

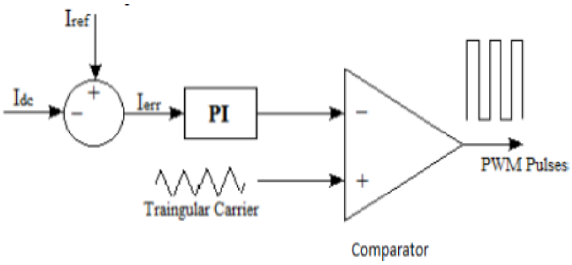

Fig. 3 Current Controller Block

III. CASCADED H BRIDGE CONVERTER

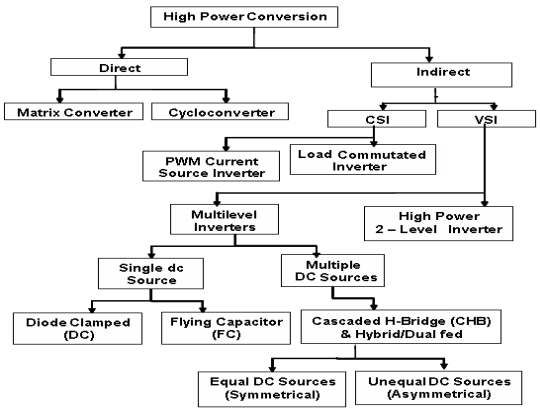

Fig.4 clasifications of power converters

The N-level cascaded H-bridge, multilevel inverter comprises ½(N-1) series connected single phase H-bridges per phase, for which each H-bridge has its own isolated dc source. Three output voltages are possible, ±Vs, and zero, giving a total number of states of $3^{½(N-1)}$, where N is odd. Figure 5 shows one phase of a n-level cascaded H-bridge inverter.

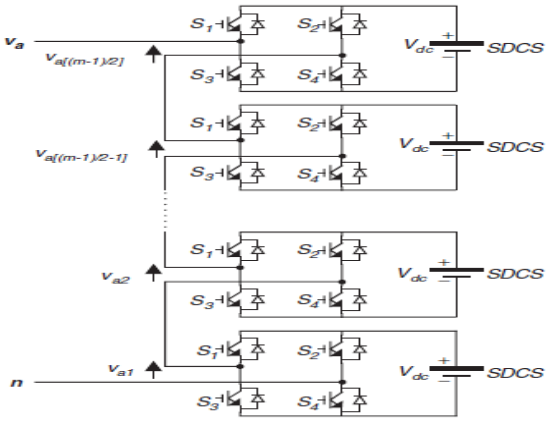

Figure 5.Single-phase structure of a multilevel cascaded H-bridge Inverter.

The cascaded H-bridge multilevel inverter is based on multiple two level inverter outputs (each H-bridge), with the output of each phase shifted. Despite four diodes and switches, it achieves the greatest number of output voltage levels for the fewest switches.

Its main limitation lies in its need for isolated power sources for each level and for each phase, although for VA compensation, capacitors replace the dc supplies, and the necessary capacitor energy is only to replace losses due to inverter losses. Its modular structure of identical H-bridges is a positive feature.

The number of levels in the line-to-line voltage waveform will be k = 2N −1. while the number of levels in the line to load neutral of a star (wye) load will be p = 2k −1.

The number of capacitors or isolated supplies required per phase is N_{cap} = ½(N −1).

The number of possible switch states is $n_{states} = N^{phases}$.

The number of switches in each leg is Sn = 2(N −1).

Advantages:

The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1).

The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages:

Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

A. Full H-Bridge- Three level inverter

Fig.6 shows the Full H-Bridge Configuration. By using single H-Bridge we can get 2 and 3 voltage levels. The number output voltage levels of cascaded Full H-Bridge inverter are given by 2n+1 and voltage step of each level is given by Vdc/n. Where n is number of H-bridges inverter connected in cascaded. The switching table is given in Table I and II.

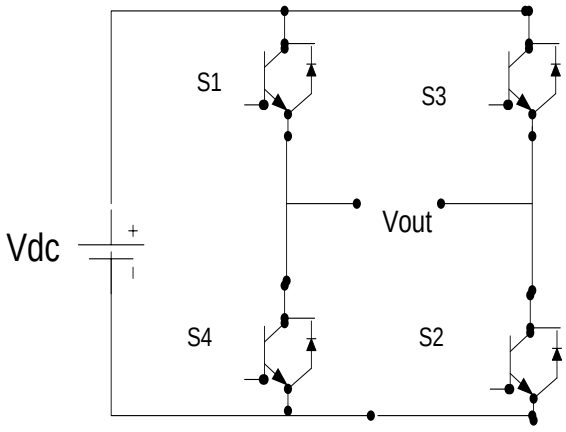

Figure 6.Full H-Bridge inverter

Table I Switching table for Full H-Bridge inverter

Switches Turn ON	Voltage Level
S1, S2	Vdc/2
S3,S4	-Vdc/2

Table II shows the Switching table for Full H-Bridge for three level inverter

TABLE II Switching table for Full H Bridge Three Level inverter

Switches Turn ON	Voltage Level
S1, S2	Vdc/2
S3,S4	-Vdc/2
S2,S4	0

B. Five level CHB Inverter

C. Figure 7 Shows the five level multilevel inverter and Table III shows the switching states of the 5 level inverter. Here even though we have eight switches at any switching state only two switches are on/off at a voltage level of Vdc/2, so switching losses are reduced. In three level inverter dv/dt is Vdc, but in five level inverter dv/dt is Vdc/2. As dv/dt reduces the stress on switches reduces and EMI reduces.

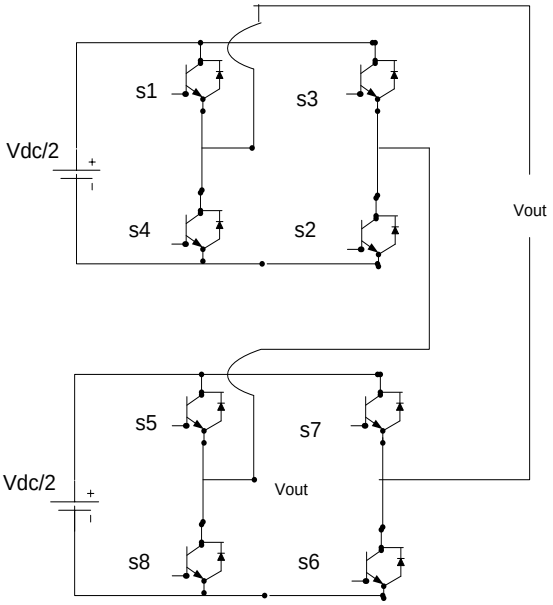

Figure.7.Five level CHB inverter

Table III Switching table for Full H-Bridge of five level inverter

Switches Turn ON	Voltage Level
S1,S2,S6,S8	Vdc/2
S1,S2,S5,S6	Vdc
S2, S4,S6,S8	0
S3,S4,S6,S8	-Vdc/2
S3,S4,S7,S8	-Vdc

D. Seven level CHB Inverter

Figure 8 Shows the seven level multilevel inverter and Table IV shows the switching states of the seven level CHB inverter.

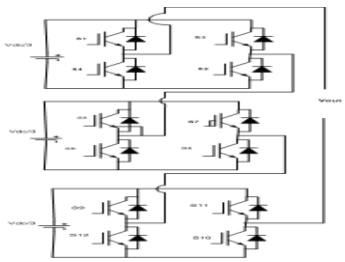

Figure 8.Seven level CHB inverter

Table IV Switching table for Full H-Bridge of seven level inverter

Switches Turn ON	Voltage Level
S1,S2,S6,S8,S10,S12	Vdc/3
S1,S2,S6,S8,S10,S12	2Vdc/3
S1,S2,S5,S6,S9,S10	Vdc
S2,S4,S6,S8,S10,S12	0
S3,S4,S6,S8 S10,S12	-Vdc/3
S3,S4,S6,S8,S10,S12	-2Vdc/3
S3,S4,S7,S8,S11,S12	-Vdc

IV. SIMULATION RESULTS

The simulation is carried out in Matlab/Simulink software and results are presented in different cases

Case-1 proposed five level inverter

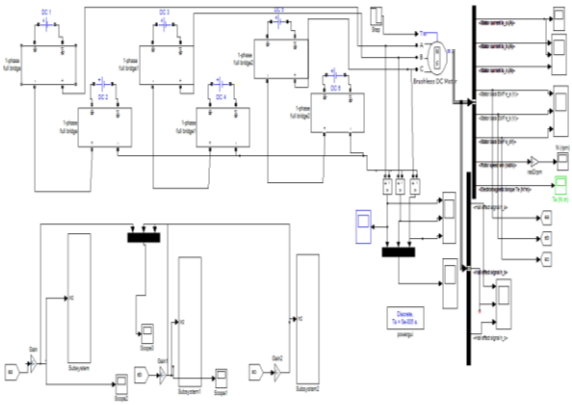

Fig.9 Matlab/simulink model of proposed five level inverter

The output of the inverter is given to the BLDC motor. The motor currents are sensed and it is given to the rectifier and the obtained value is compared with the reference value and the error value is processed using PI controller. The obtained value is compared with the triangular wave to generate controlled PWM signals The motor currents are sensed and it is given to the rectifier and the obtained value is compared with the reference value and the error value is processed using PI controller. The obtained value is compared with the triangular wave to generate controlled PWM signals. The obtained pulses are taken from position sensor signals of the motor to give pulses to multilevel inverter.Fig.6 shows the output signal from the Hall Effect sensor of the Brushless DC motors

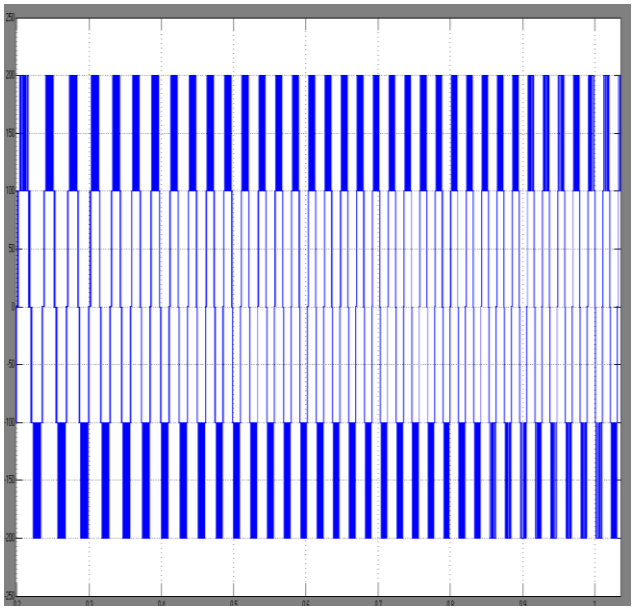

Fig. 10 phase to phase voltage of BLDC motor

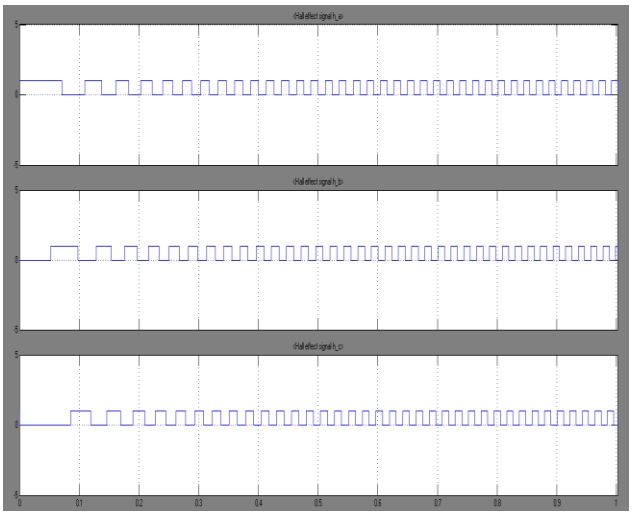

Fig.11 output of Hall Effect sensors

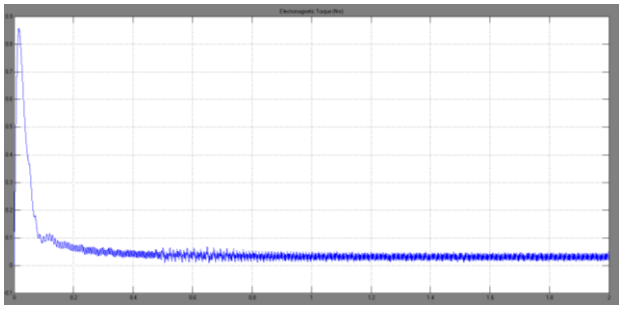

Fig. 12 Torque waveform of BLDC motor

The Fig.8 which shows the FFT analysis of the Phase A current of the Brushless DC motor. it is found that THD is 5.44%

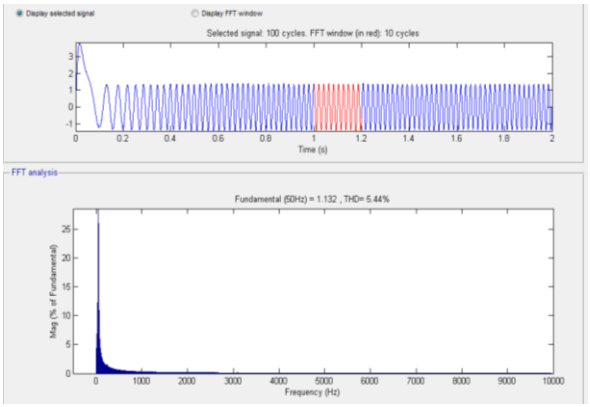

Fig. 13 FFT analysis of phase current A is 5.44%

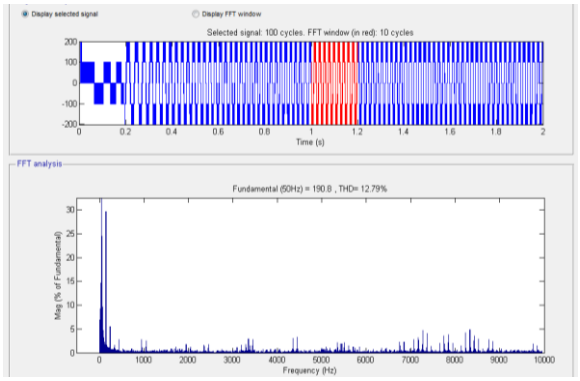

Fig. 14 FFT analysis of phase voltage

The Total Harmonic Distortion (THD) which tells the amount of harmonics present in the current or voltage. In above figure shows the FFT analysis of the Phase-Phase voltage of the Brushless DC motor. The amount THD also calculated for this waveform. is 12.79%

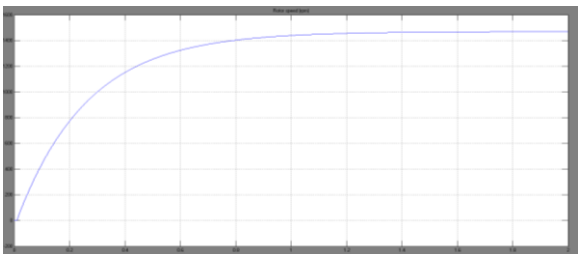

Fig. 15 speed of BLDC motor

Fig.15 shows the speed waveform of Brushless DC motor. The harmonics and the torque ripple can be reduced by smoothening the current waveform.

Case-2 seven level inverter fed BLDC motor

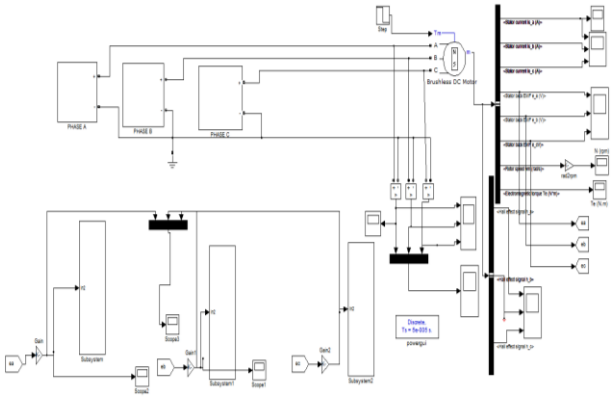

Fig.16 seven level inverter fed BLDC motor

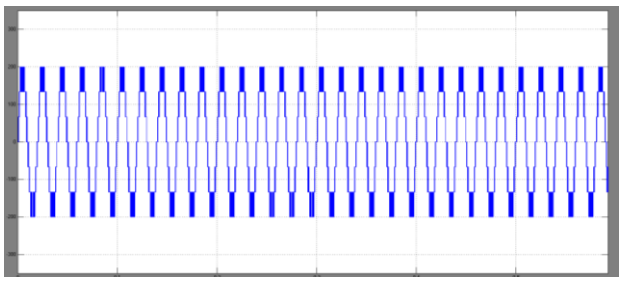

Fig. 17 phase to phase voltage of 7-level BLDC motor

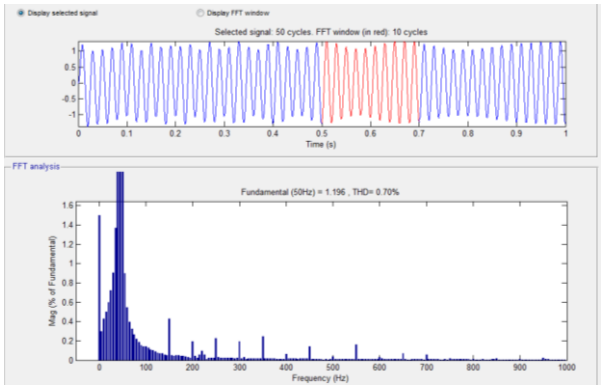

Fig. 18 FFT analysis of phase current A is 0.7%

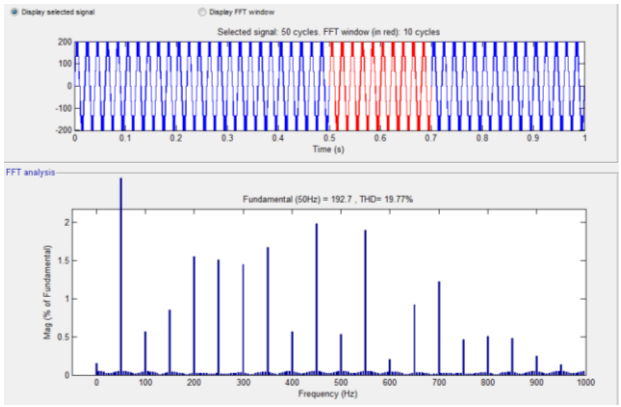

Fig. 19 FFT analysis of phase voltage is 19.77%

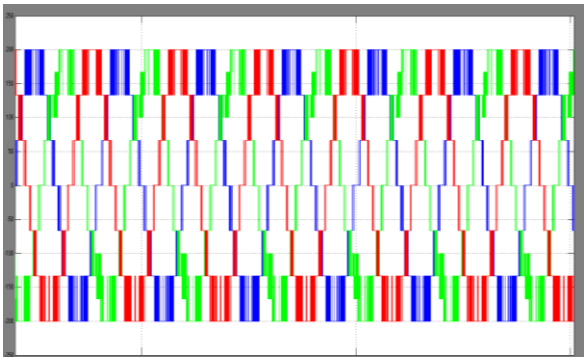

Fig. 20 three phase output voltage of 7-level BLDC motor

V. CONCLUSION

This paper has given a brief summary of different types of multilevel inverters and their circuit topologies. Today, more number of and more commercial products are based on the multilevel inverter structure. This paper has proposed harmonics and torque ripples have been reduced using multilevel inverter with the current controlled technique. The harmonics content of the voltage and Current for a BLDC motor is analyzed and the amount of torque ripple and the THD also calculated. The main advantage of this method is it uses one current controller for the three phases. Finally a generalized expression for highest order harmonic based on switching frequency and number of levels is derived. Matlab/Simulink models are developed.

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