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RESEARCH ARTICLE

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LOW POWER AND HIGH SPEED BRENT-KUNG ADDER

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ABSTRACT

Parallel-prefix adder (BK) offers a highly-efficient solution to the binary addition problem. Since Parallel Prefix Adders have been established as the most efficient circuits for binary addition .Their regular structure and fast performance makes them particularly attractive for VLSI implementation .The VLSI implementation results show a significant delay reduction and area x time2 improvements, all this at the cost of high power consumption, which is the main reason for preventing the use of parallel prefix Kogge Stone adder. To solve this problem Parallel Prefix based Brent Kung Adder components provides a better tradeoff between power and area.

Key Words—Digital Arithmetic, Parallel Prefix Adder, Residue number system, Reverse Converter

INTRODUCTION

In the world of battery-based and portable devices, the residue number system (RNS) can play a significant role due to its low power features and competitive delay. The RNS can provide carry free and fully parallel arithmetic operations for several applications, including digital signal processing and cryptography. However, its real usage requires forward and reverse converters to be integrated in the existing digital systems. The reverse conversion, i.e., residue to binary conversion, is a hard and time-consuming operation. Hence, the problem of designing high-performance reverse converters has motivated continuous research using two main approaches to improve the performance of the converters:

1) Investigate new algorithms and novel arithmetic formulations to achieve simplified conversion formulas

2) Introduce new moduli sets, which can lead to more simple formulations. Thereafter, given the final simplified conversion equations, they are computed using well-known adder architectures, such as carry-save adders (CSAs) and ripple-carry architectures, to implement carry-propagate adders (CPAs) and, more seldomly, fast and expensive adders such as the ones with carry-look ahead or parallel-prefix architectures.

In this brief, for the first time, we present a comprehensive methodology to wisely employ parallel-prefix adders in carefully selected positions in order to design fast reverse converters. The collected experimental results based on area, delay, and power consumption show that, as expected, the usage of the parallel-prefix adders to implement converters highly increases the speed at the expense of additional area and remarkable increase of power consumption. The significant growing of power consumption makes the reverse converter not

competitive. Two power-efficient and low-area hybrid parallel-prefix adders are presented in this brief to tackle with these performance limitations, leading to significant reduction of the power delay product (PDP) metric and considerable improvements in the area-time2 product (AT2*)* in comparison with the original converters without using parallel-prefix adders

BACKGROUND

The forward converter, modulo arithmetic units, and reverse converter are the main parts of the RNS. In contrast to other parts, reverse converter consists of a complex and no modular structure. Therefore, more attention should be directed to its design to prevent slow operation and compromise the benefits of the RNS. Both the characteristics of the moduli set and conversion algorithm have significant effects on the reverse converter performance. Hence, distinct moduli sets have been introduced. In addition to the moduli set, hardware components selection is key to the RNS performance. For instance, parallel-prefix adders are known as unsuitable structures for complex reverse converters because of their high power consumption. However, parallel-prefix adders with its high-speed feature have been used in the RNS modular arithmetic channels. This performance gain is due to parallel carry computation structures, which is based on different algorithms .Each of these structures has distinct characteristics, such as Sklansky (SK), and Kogge–Stone (KS) have the maximum and minimum fan-out, respectively, both providing minimal logic depth. Minimum fan-out comes at the expense of more circuit area. Therefore, hardware components selection should be undertaken carefully.

KOGGE STONE ADDER

KSA is a parallel prefix form carry look ahead adder. It generates carry in O (logn) time and is widely considered as the fastest adder and is widely used in the industry for high performance arithmetic circuits. In KSA, carries are computed fast by computing them in parallel at the cost of increased area.

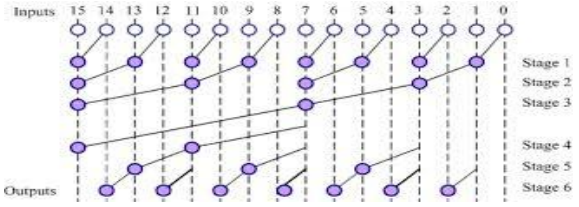

Fig.1. Kogge Stone Adder

NEW-PARALLEL-PREFIX-BASED COMPONENTS (BK)

The Chinese remainder theorem, or other related improved approaches and techniques underlie the RNS reverse conversion, whose formulation can be directly mapped to ripple-carry adders (RCA). However, this leads to significant speed degradation, due to the linear increase of the delay in the RCA with the number of bits. Parallel-prefix adders can be used in the RNS reverse converters to bind the delay to logarithmic growth. However, in reverse converters, several parallel-prefix adders are usually required. Even when only one adder is used, the bit length of this adder is quite large.

Consequently, this results in high power consumption notwithstanding its high speed. Therefore, in this section, two approaches that take advantage of the delay properties of the parallel prefix adders with competitive power consumption are introduced. Usually, one regular binary addition is required in reverse converter structures to achieve the final binary representation. This final addition has an important effect in the total delay of the converter due to the large bit-length of the operands.

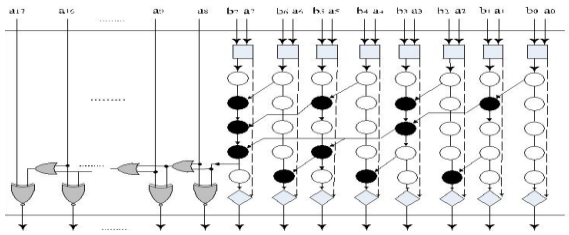

Fig.2. HRPX structure with BK prefix network

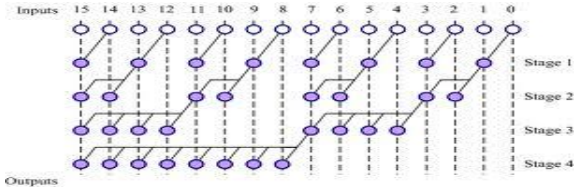

Fig.3. Parallel Prefix based Brent Kung Adder

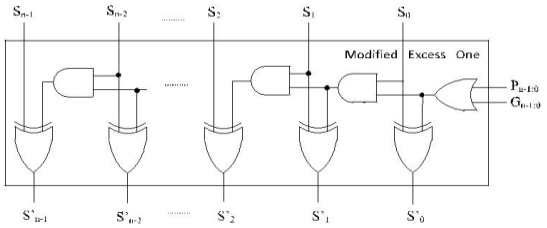

Fig.4. Modified Excess-one unit

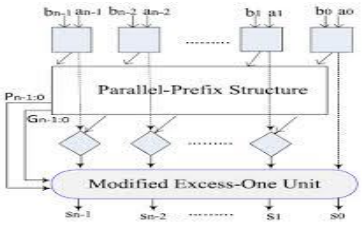

Fig.5. HMPE Structure

REVERSE CONVERTER DESIGN METHODOLOGY

In this section, the methodology of reverse converter design is described. In the following, a method employing distinct components in the architecture of the reverse converter will be presented. Several reverse converters for different moduli sets have been introduced, which can be classified into three classes. The first class consists of converters with a tree of CSAs with EAC followed by a two-operand modulo $2^k - 1$ CPA [8], [10]. A second class includes more complex reverse converters, which have several CSAs and CPAs with EACs followed by a final regular subtractor with two operands of different size [10]–[12]. The implementation of this subtractor using regular binary-adder results in one operand with some constant bits. The third class covers the reverse converters that have been designed for moduli sets with moduli other than the popular 2^n and $2^n \pm 1$ [14].

COMPARISIONS

Tables 1 and 2 show the results for the moduli set $\{2^n - 1, 2^n, 2^n + 1, 2^{2^{n+1}} - 1\}$ converters. As it was expected, the RCA-based converter [10] suggests the most competitive area and the power consumption metrics, but the highest delay. The suggested designs have considerably improved the delay, AT^2, and PDP while slightly increasing the area. Although, more power was consumed, the balance between power and delay becomes more competitive when the PDP metric is adopted. By comparing with the converter using fully parallel-prefix adders, the area, power, AT^2 (except at $n = 4$), and PDP of the proposed designs are significantly improved, but the delay increases. Experimental results for the converters with moduli-set $\{2^n - 1, 2^n + 1, 2^{2n}, 2^{2n+1} - 1\}$ are presented in Tables 3 and 4. Similar behavior is observed except for the PDP metric. The PDP for the proposed converters are worse than for the RCA based [11] in three cases, but this improves for larger values of n, even for n = 16 the HMPE and HRPX-SK structure has better PDP than the RCA-based one.

Our main goal is to decrease the cost of achieving high speed converters using parallel-prefix adders and also to provide applicable competitive tradeoff between power consumption and delay. For instance, with the HMPE and HRPX-SK converter for n = 16%, 63% of the power is saved at the expense of 35% delay increase, and also 42% of improvement in the PDP is achieved when compared with fully parallel-prefix adders based designs. In the other hand, the proposed designs consume more power to achieve higher speed than the RCA-based ones.

TABLE.1. Experimental results for moduli $\{2^n - 1, 2^n, 2^n + 1, 2^{2n+1} - 1\}$ converters

Converter 1	Chip Area (μm^2)				Useful Area(μm^2)				Delay (ns)			
Structure	4	8	12	16	4	8	12	16	4	8	12	16
RCA-based Adders	4199	8359	12137	17029	1402.6	2904.5	3918.2	5257.1	0.64	1.02	1.394	1.766
Fully Prefix Adders	5476	10774	18140	23741	1720.8	3589.9	6111.7	8435.2	0.324	0.505	0.515	0.565
HMPE & HRPX-KS	4873	10547	16348	22616	1591.6	3476.5	5797.1	7873.9	0.456	0.545	0.593	0.61
HMPE & HRPX-SK	4292	8853	12902	17739	1440.4	2842.2	4292.3	6188	0.474	0.53	0.579	0.626
HMPE & HRPX-BK	4199	8392	12746	16596	1458	2947	4367.5	5991.5	0.438	0.548	0.614	0.624

TABLE.2. Comparing power, at^2 and PDP for moduli $\{2^n - 1, 2^n, 2^n+1, 2^{2n+1} - 1\}$ converters

Converter 1	Power (mW)				AT^2				PDP			
Structure	4	8	12	16	4	8	12	16	4	8	12	16
RCA-based Adders	3.631	4.534	5.004	5.447	574.50	3021.84	7613.99	16395.61	2.32	4.62	6.98	9.62
Fully Prefix Adders	9.522	11.64	18.54	24.18	180.64	915.51	1620.98	2692.73	3.09	5.88	9.55	13.66
HMPE & HRPX-KS	5.373	9.595	14.4	18.72	330.95	1032.61	2038.54	2929.88	2.45	5.23	8.54	11.42
HMPE & HRPX-SK	4.635	8.389	10.87	13.97	323.62	798.37	1438.95	2424.93	2.20	4.45	6.29	8.75
HMPE & HRPX-BK	5.055	8.148	10.74	14.44	279.71	885.00	1646.53	2332.95	2.21	4.47	6.59	9.01

TABLE.3. Experimental results for moduli $\{2^n - 1, 2^n + 1, 2^{2n}, 2^{2n+1} - 1\}$ converters

Converter 2	Chip Area (μm^2)				Useful Area(μm^2)				Delay (ns)			
Structure	4	8	12	16	4	8	12	16	4	8	12	16
RCA-based Adders	4639	9858	13710	17901	1575.7	3223.8	4347.7	5638	0.693	1.056	1.33	1.736
Fully Prefix Adders	6674	12972	22350	29100	2259	4597.9	7729.6	10480.7	0.43	0.485	0.54	0.578
HMPE & HRPX-KS	5898	12655	20218	27783	1960.9	4376.5	6775.9	9753.8	0.472	0.577	0.607	0.667
HMPE & HRPX-SK	4873	10181	14639	18413	1661	3208.7	5267.5	6304.3	0.489	0.595	0.593	0.689
HMPE & HRPX-BK	4873	9999	13686	19207	1708.2	3417.8	4965.1	6684.1	0.451	0.577	0.646	0.659

TABLE.4. Comparing power, at^2 and PDP for moduli $\{2^n - 1, 2^{2n}, 2^n+1, 2^{2n+1} - 1\}$ converters

Converter 2 Structure	Power (mW)				AT^2				PDP			
	4	8	12	16	4	8	12	16	4	8	12	16
RCA-based Adders	3.615	4.528	5.485	5.761	756.73	3594.98	7690.65	16991.22	2.51	4.78	7.30	10.00
Fully Prefix Adders	9.104	17.41	26.31	34.22	417.69	1081.54	2253.95	3501.43	3.91	8.44	14.21	19.78
HMPE & HRPX-KS	6.879	12.05	17.34	24.83	436.86	1457.06	2496.57	4339.36	3.25	6.95	10.53	16.56
HMPE & HRPX-SK	5.94	8.522	13.28	13.56	397.18	1135.96	1852.31	2992.78	2.90	5.07	7.88	9.34
HMPE & HRPX-BK	5.916	9.152	11.72	15.17	347.45	1137.88	2072.02	2902.78	2.67	5.28	7.57	10.00

SIMULATION RESULTS

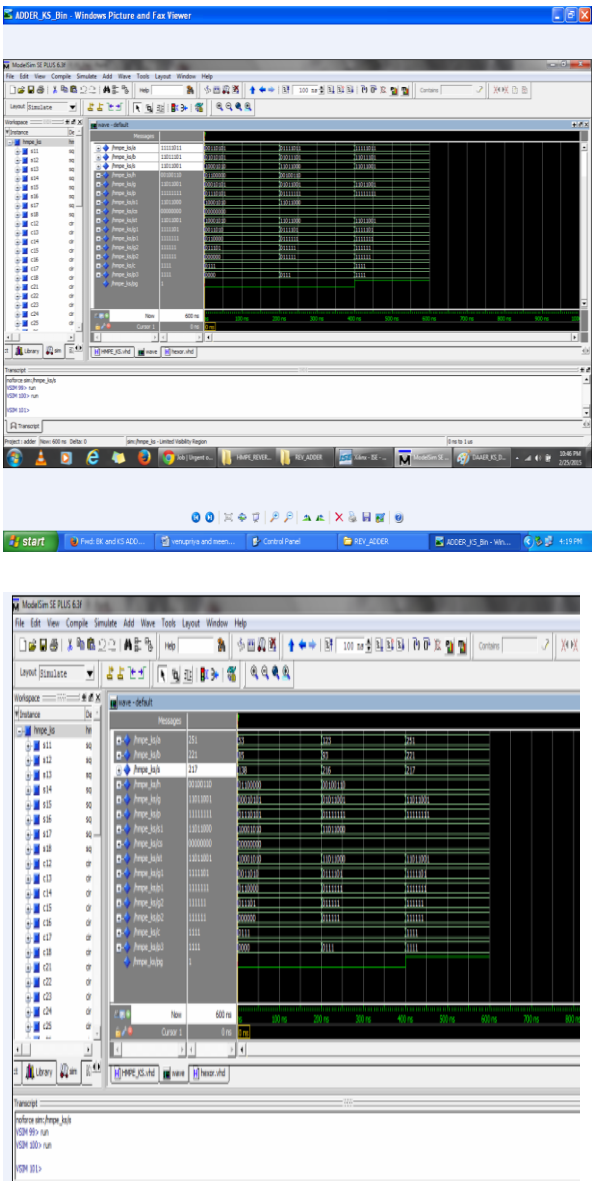

Fig.6. Waveforms of BK Adder

CONCLUSION

This brief presents a method that can be applied to most of the current reverse converter architectures to enhance their performance, cost and area. Furthermore, in order to provide the required tradeoffs between cost and area, Parallel Prefix based Brent Kung Adder components were introduced. These components are specially designed for reverse converters. Implementation results show that the reverse converters based on the suggested components considerably improve the speed when compared with the original converters, which do not use any parallel-prefix adder, and reduce the power consumption compared with the converters that exclusively adopt parallel-prefix adders.

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