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RESEARCH ARTICLE

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PERFORMANCE ANALYSIS OF CASCADED H-BRIDGE MULTILEVEL INVERTER USING DC SOURCES

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ABSTRACT
In this paper, cascaded H-bridge Multilevel inverter is proposed to determine the magnitude of dc voltage source and to achieve high output voltage level by using less number of components. Multilevel inverter is used to generate higher power with a series of power semiconductor switches with several low voltage dc source to perform the power conversion. Cascaded H- bridge inverter is connected in series to provide a sinusoidal output voltage. Each cell contains one H-bridge and output voltage generated by this multilevel inverter is actually sum of all the voltage generate each cell. If there are k level in a cascaded H- bridge multilevel inverter then number of level will be 2k+1. Cascaded H- bridge inverter has advantage over other types of multilevel inverter when compared it requires less number of components and it is of low cost. Output voltage level is doubled. The proposed multilevel inverter control is done by PIC controller. The accuracy performance of the proposed inverter can be verified through the experimental results on a 31 level inverter.
Keywords— Cascaded multilevel inverter; H-bridge cascaded inverter; power electronic devices; PIC controller

I.INTRODUCTION

There are different problem in semiconductor devices independently in high voltage and high power application such as limitation in current generation, impossibility of connected to grid directly etc. Multilevel inverter have become more popular over the years in industrial application and high power application with promise of less disturbance, smaller common mode voltage, the possibility to function at lower switching frequency, and good potential for further development than ordinary two level inverter.[1][2] Though conventional two level inverter are effective , but create harmonic distortion in the output voltage, EMI and high dv/dt compared to multilevel inverter. As a result, the most attractive application of multilevel inverter are in the medium to high voltage ranges. The concept of multilevel inverter does not depend up on the two level of voltage to create an AC signal. Instead of several voltage level are added to each other to create a smoother waveform with lower harmonic distortion. with more voltage level of inverter , the waveform become smoother but with many level the design become more complicated, with more components . A multilevel inverter not only achieve high power rating, but also enables use of renewable energy sources such as photovoltaic, wind, and fuel cells

can be easily interfaced to a multilevel inverter system for high power application. Recently, in order to generate higher quality output wave form, reduce the number of power electronics device, cost and installation space of the inverter. Many research on new control methods and topologies of the multilevel inverter have been done. From the different types of multilevel inverter are flying capacitor, neutral point clamped, cascaded H-bridge. Among these topologies, the cascaded H-Bridge inverter has much attention. The advantage of cascaded H-bridge inverter are require less number of components per level, Modularized structure without clamping components, possibility to implement soft switching. The proposed topology is of cascaded multilevel inverter with asymmetrical configuration, since it used several levels of DC voltage, which would be available from batteries, ultra capacitor or fuel cells. Because of these several levels of DC sources may cause voltage imbalance which leads to the increase of harmonic and total harmonic distortion. The proposed topology shows how to operate this convertor in order to maintain equal charge/ discharge rates from the DC sources. This is called pulse width modulation in the multi level inverter.[2] With this technique the harmonic content is also reduced since switching frequency is restricted by switching losses in high power and high voltage application, multilevel inverter have found vide acceptance as they can achieve a low harmonic component with low switching frequency. Furthermore, low blocking voltage by switching devices is the other advantage of this type of inverter as well as minimum harmonic distortion and switching loses. The blocked voltage by each switch in a specific unit is same as the other switches used in same unit and is equal to the magnitude of DC voltage sources used in the unit. Therefore, the number of gate driving circuit is reduced and as a result the size of multilevel inverter and its power consumption are reduced. Another feature of the proposed topology is there is many kind of necessity to bidirectional switches.[3] In this paper a new procedure is recommended to find out the magnitude of DC voltage sources and produce all output voltage level. Finally a method to find out the Optimum number of switches and DC voltages so that have the maximum output voltage level with the minimum blocked voltage by switches is presented.[1][3].

II. VOLTAGE BALANCING TECHNOLOGY

Asymmetric multilevel inverters have the same topology as symmetric multilevel inverters. They differ only in the rating of input dc voltages and control strategies. For many applications it is troublesome to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. which uses lesser number of bridges.[3] This scheme therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency. Although the cascaded converter has an inherent self-balancing characteristic, a slight voltage imbalance can occur because of the circuit component losses[5][6]. The most important factors causing the voltage imbalance among these DC capacitors are the difference in the power stage losses and the component tolerances.[5] The internal losses may be differently influenced by the switching and conduction activity and the component tolerances. To achieve steady-state, balanced voltage, these DC capacitors must have the same amount of real power utilization in a given period of time.[4]. Due to sharing the same output current, the differences in the capacitor currents are caused by the different duty cycles, because a capacitor current is a product of a duty cycle and an output current. Therefore, the average switching functions or duty cycles in these H-bridge converters must be identical.

III. PROPOSED TOPOLOGY

The proposed multilevel inverter not only has the modularity features of cascaded topologies but consists of the ability of series and parallel connection of dc voltage source. Each unidirectional power switches consists of an IGBT with an antiparallel power diode and a driver circuit. Therefore in the basic unit, the number of switches are equal to number of power diodes [1][4]. Therefore, in the basic unit, the number of switches

(Nswitch) is equal to the number of power diodes (Ndiode) , IGBTs (N IGBT) and driver circuits where m is the number of the dc voltage sources on each leg.[1] the output voltage of the basic unit for different switching state [4][5]. As it is obvious from Table I, this unit is able to generate all positive and negative levels at the output. The magnitude of dc voltage source are different from one unit to another. The power switches of (SL1 and SL2) should not turned turn on simultaneously because of avoiding short circuit across the dc voltage source VL1,VLn,VR1,VRn…In order to increase the number of output voltage level, it is possible to connect n number of proposed unit to generate new cascaded H-bridge multilevel inverter.[7] In the proposed cascaded multilevel inverter, the number of used dc voltage source is the first, second and nth basic unit is generally equal to 2m1,2m2 and 2mn respectively[1][5].

IV. PRINCIPLE OF OPERATION

The required dc voltage source in the proposed multilevel inverter may be available through renewable energy sources such as batteries [5] .the dc voltage source should have unequal value, called asymmetrical cascaded inverter. In this proposed topology using asymmetrical multilevel inverter [6][5]. In order to increase the number of output voltage levels and reduce the number of power switches, driver circuits, and the total cost of the inverter, a new topology of cascaded multilevel inverters is proposed[2],[4],[7] and [8].Then, to determine the magnitude of the dc voltage sources. Moreover, the proposed topology is compared with other topologies from different points of view such as the number of switches, number of dc voltage sources, the variety of the values of the dc voltage sources, and the value of the blocking voltages per switch. Finally, the performance of the proposed topology in generating all voltage levels through a 31-level inverter is confirmed by simulation using matlab/simulink. The proposed topology of multilevel inverter for 31 level inverter shown in figure.1.

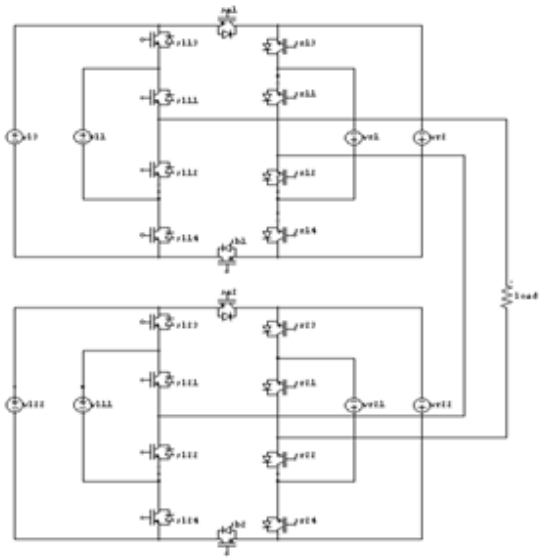

Fig.1.Proposed topology.

It consists of four bridges that are two upper bridge and two lower bridge with series circuit, which are cascaded. In a conventional cascaded multilevel inverter the number of output phase voltage level is defined by n=2m+1, where m is the number of dc voltage sources.[9] Each H-bridge requires a dc voltage sources and four switches. Twelve switching devices are needed for 7 level and sixteen switching are needed for 9 level and fourty switches are needed for 21 level, which makes an inverter complicated. In multilevel inverter using 31 level is required 20 switches, when compared to conventional inverter, it has less number of switches are required in more number of level [8][10] . The advantage of this inverter reduced the number of switches and also reduced the harmonics means of increase the level of inverter.

But the proposed inverter outputs 12n+7 levels, where n is number of basic unit in cascaded multilevel inverter. Total number of switching devices required is 3n+14, which makes the output voltage of the inverter almost sinusoidal [7]. Figure.3.shows the proposed topology for 31 level output, it consists of two voltage sources in the series circuit. Switching sequence of 31 level, which is shown in table.2. This unit is able to generate all positive and negative level at the output voltage. For this selection , the maximum number of level of output voltage level , maximum number of dc

source and number of switches can be determined by the following equation.

V. SWITCHING MODE

The proposed inverter are combined of unidirectional power switches (sa, sb, sl1, sr1, sr2, sr3, sr4, sl3, sl4) and four dc voltage sources (vl1, vl2, vr1, vr2) is the first basic unit.

Switches (sa1, sb1, sr5, sr6, sl5, sl6, sl7, sl8, sr8, sr7) and four dc voltage sources (vl3,vl4,vr3,vr4) is the second basic unit which are cascaded. simultaneously turn on sl1,sl2 or sl3,sl4 is cause the voltage across to short circuit. So the switches do not turn on at a time.

Table:1.Switching sequence of proposed topology

Vo	SWITCHES ARE CLOSED
VL1	Sl1,sl4,sr2,sr4,sb1,sb2,sl6,sl8,sr6, sr8
VR1	Sl2,sl4,sr1,sr4,sb1,sb2,sr8,sr6,sl6, sl8
VL2	Sl1,sl3,sr1,sr4,sb1,sl5,sl7,sr6,sb2
VR2	Sl2,sl4,sr1,sr3,sb1,sb2,sr7,sr1,sl6, sl8
VL3	Sl5,sr2,sr4,sb1,sl4,sl2,sr6,sr8,sb2, sl8
VR3	Sr8,sb1,sl8,sl6,sr2,sr4,sb2,sl4,sl2, sr5
VL4	Sl7,sl5,sr2,sr4,sb1,sl4,sl2,sr6,sr8,sb2
VR4	Sb2,sl8,sl6,sr2,sr4,sb1,sl4,sl2,sr7, sr5
Zero	0
-VR4	Sa2,sl7,sl5,sr1,sr3,sa1,sl3,sr8,sr6
-VL4	Sl8,sl6,sr1,sr3,sa1,sl3,sl1,sr5,sr7, sa2
-VR3	Sr7,sa1,sl7,sl5,sr1,sr3,sa2,sl3,sl1, sr6
-VL3	Sl6,sr1,sr3,sa1,sl3,sl1,sr5,sr7,sa2, sl7
-VR2	Sl1,sl3,sr2,sr4,sa1,sa2,sr8,sr2,sl5, sl7
-VL2	Sl2,sl4,sr2,sr3,sa1,sl6,sr8,sr5,sa2
-VR1	Sl1,sl3,sr1,sr3,sa1,sa2,sr7,sr5,sl5,sl7
-VL1	Sl2,sl3,sr1,sr3,sa1,sa2,sl5,sl7,sr5,sl7

Mode:1

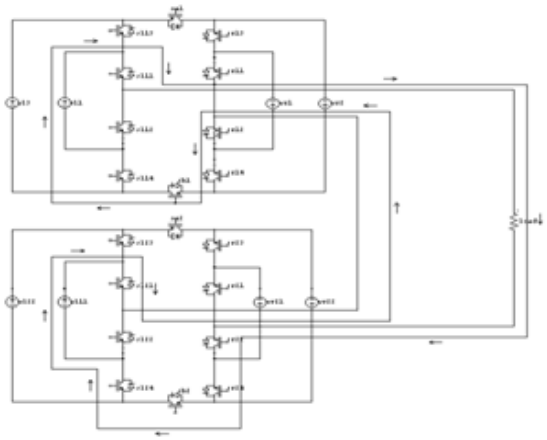

Fig.2.Switching sequence for getting a voltage of („VL1").

For positive voltage vl1 voltage level sl1, sl4, sr2, sr4, sb1, sl6, sl8, sr6, sr5 are switched on for getting a maximum voltage. In this switching conduction is trigger by pulse generation signal to generate the output voltage as high.

Mode:2

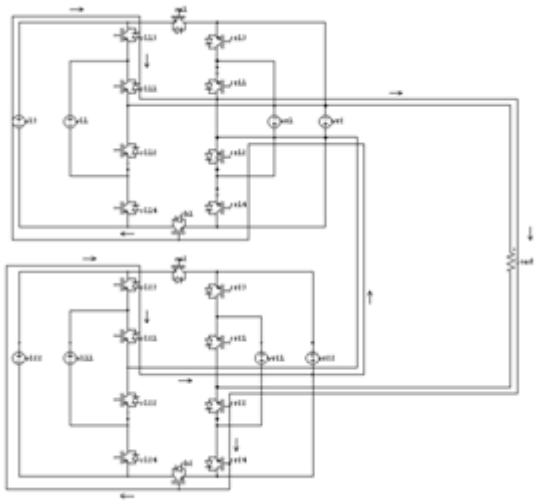

Fig.3. Switching sequence for getting a voltage(„VL2").

For positive voltage vl2 voltage level sl3,sl1,sr6,sr8,sb1,sl7,sl5,sr6,sr8,,sb1 are switched on and other switches are open state for getting maximum voltage .

Mode:3

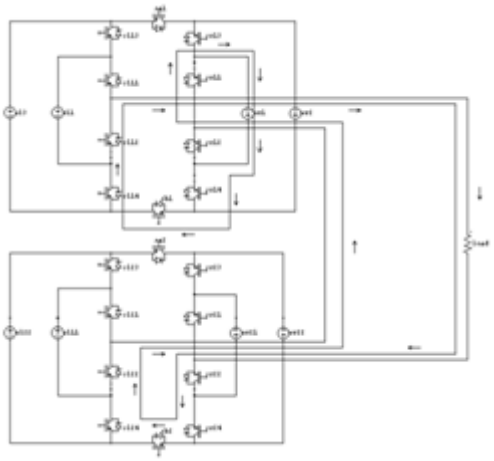

Fig .4.switching sequence for getting a voltage(vr1)

For positive voltage of right side voltage level sr1,sr2,sr4,sl4,sb1,,sb,sr8,sr6,sl8,sl6 are switched on for getting maximum voltage. Signal is given to the switch for triggering to send command signal to switching devices.

Mode:4

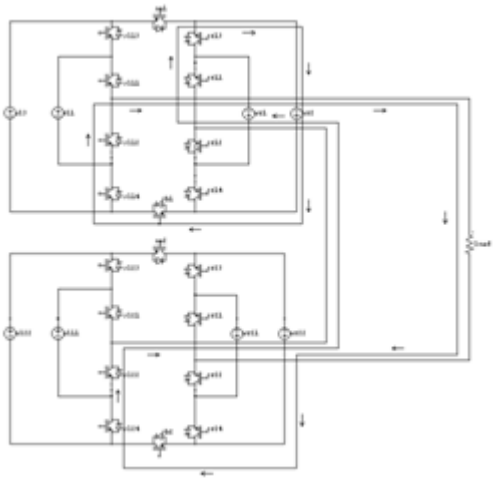

Fig .6.Switching sequence for getting a voltage(„vr2")

For positive voltage of right side voltage level sl2,sl4,sb,sb1,sr6,sr8,sr1,sr3 are switched on for getting maximum voltage.

VII.COMPARISON WITH CONVENTIONAL METHOD

The main aim of presentation the proposed cascaded multilevel inverter is increasing the number of output voltage levels by using lower number of power electronic devices. In order to investigate the feature the proposed cascaded multilevel inverter is compared with the conventional cascaded inverters from the amount of blocked voltage by switches, the number of required power switches and dc voltage sources points of view.[1][2]

Table.2.Comparison with conventional inverter

LEVEL	DC SOURCE	SWITCH
21	10	40
31	8	20

VI.DESIGN AND ANALYSIS

The matlab/ simulink model of the proposed inverter for 31 level output is shown in figure.7. It consists of one H-bridge are cascaded with lower H-bridge of circuit .simulation is performed for the proposed circuit with MATLAB.

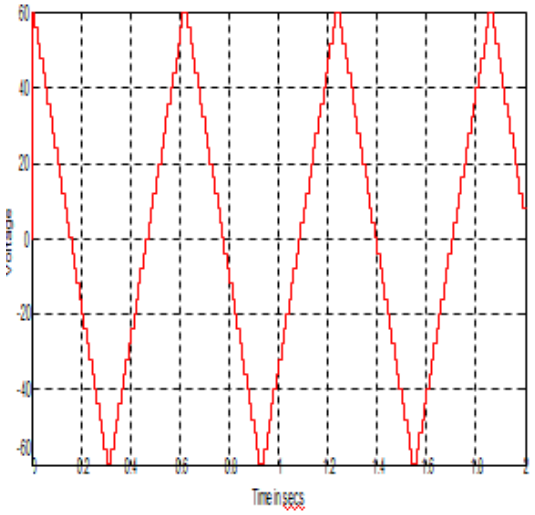

Fig.7.Simulation result.

Matlab/ simulink model for 31 level output 2V for VL1, 10V for VL2 and the two voltage sources of circuit are 24 V each maintaining the ratio 1:5:12, then the amplitude of the inverter output voltage waveform for 31 level is to 60 Vac.

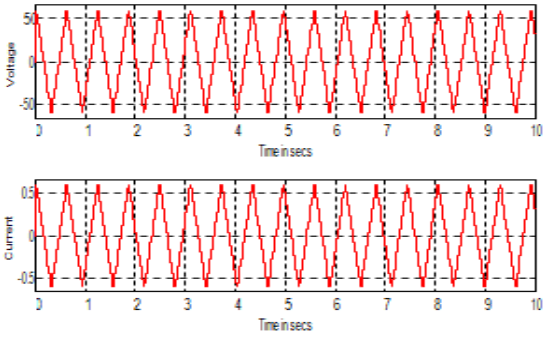

Fig.8. Output voltage and current waveform.

Figure.8. shows the 31 level output voltage and current waveform without pulse width modulation. It is clear that as the number of level increases, distortion reduces. Switch required is the proposed topology compared to other topology.

VIII. HARDWARE DESIGN

The required dc voltage source are obtained from the renewable energy sources such as batteries. When an ac voltage is already available multiple dc voltage sources can be generated using transformer .The hardware system of the proposed converter is implemented using a PIC microcontroller. The software system like Proteus, Mplab, and Micropro is used for the system design for coding the pulses in to the PIC controller. The power supply circuit is designed that will control the PIC and driver circuit to drive the pulses to the MOSFET. Power supply unit for PIC 16F877A microcontroller This section describes how to generate +5V DC power supply and +12V DC power supply by step down transformer(0- 12v).

Fig .9. Hardware design.

IX.PIC MICROCONTROLLER

Microcontroller (sometimes abbreviated µC, uC or MCU) is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals. Program memory in the form of NOR flash or OTP ROM is also often included on chip, as well as a typically small amount of RAM. Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications. PICs are popular with both industrial developers and hobbyists alike due to their low cost, wide availability, large user base, extensive collection of application notes, availability of low cost or free development tools, and serial programming (and re-programming with flash memory) capability. The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also known as a Serial Communications Interface or SCI.) The USART can be configured as a full-duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers, or it can be configured as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs, etc. Microcontrollers are used in automatically controlled products and devices, such as automobile engine control systems, implantable medical devices, remote controls, office machines, appliances, power tools, toys and other embedded systems. By reducing the size and cost compared to a design that uses a separate microprocessor, memory, and input/output devices, microcontrollers make it economical to digitally control even more devices and processes. Mixed signal microcontrollers are common, integrating analog components needed to control non-digital electronic systems.

X.CONCLUSION

Cascaded multilevel inverters is used to improve the efficiency in addition to acceptable reliability and simple control, provide a better voltage waveform than the other types of multilevel inverters. In this paper, a new cascaded multilevel inverter topology was proposed which was connected to the dc voltage sources in series and parallel. The suggested topology needs less number of switching devices with minimum standing voltage. THD is also reduced without using modulation techniques. And the proposed topology shows how to operate the Cascaded multilevel inverter without any voltage unbalance problems. The simulation results are verified through 31 level inverter which are accorded with the theoretical results. The

proposed inverter is used in high power applications like EV and industries.

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