International Journal of Engineering Research-Online
A Peer Reviewed International Journal
Articles available online http://www.ijoer.in; editorijoer@gmail.com

Vol.4., Issue.6., 2016
Nov-Dec.

RESEARCH ARTICLE

ISSN: 2321-7758

'SOLS' ARCHITECTURE BASED DESIGN OF FM0/MANCHESTER ENCODER AND IMPLEMENTATION ON 'FPGA'

MINAKSHI SHARMA[1], NEETESH RAGHUWANSHI[2], MANISH JAIN[3]

[1,2]Department of Electronics and Instrumentation

[3]Department of Electronics and Communication

[1,2,3] RKDF-IST, Hoshangabad Road, Bhopal

[1]minakshi786@gmail.com;[2]neeteshrkdf2010@gmail.com;[3]manishj.mitece@gmail.com

ABSTRACT

(DSRC) abbreviated as dedicated short-range communication is associate as the rising technique to push the intellectual installation into existing ones. Some of the problem such as DC-balance, enhancement of signal irresponsibleness is successfully handled by FM0 and Manchester codes that are the standard for DSRC. The coding-diversity between the FM0 and Manchester codes becomes the serious area to work which seriously limits the potential to reused VLSI design. In this paper, the similarity-oriented logic simplification (SOLS) technique is projected to strike this limitation. SOLS is a technique that improves the hardware utilization rate at some present for each FM0 and Manchester encodings. The coding capability of this paper will totally support the DSRC standards of America, Europe, and Japan. This paper not solely develops a completely reused VLSI design, however additionally exhibits Associate in tending economical performance compared with the established works and also implement the outcome of the technology with the help of FPGA.

INTRODUCTION

The dedicated short range communication is a protocol for one or two way medium range communication. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to roadside. In automobile-to-automobile, the DSRC enables the message sending and broadcasting among automobile. The automobile-to roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC). The DSRC architecture having the transceiver. The microprocessor is used to transfer the instruction to the baseband processing and RF front end. The RF front end is used to transmit and receive the wireless signals using the antenna. The baseband processing is responsible for modulation, error correction, encoding and synchronization. The transmitted signal consists of the arbitrary binary sequence; it is very difficult to obtain the dc-balance. The fm0 and Manchester is providing the transmitted signal and then the dc-balance. The (SOLS) similarity oriented logic simplification having the two methods: area compact retiming and balance logic operation sharing. The area compact retiming used to reduce the transistor counts .the balance logic operation sharing is used to combine the fm0 and Manchester encoding. All the bits of the binary data in Manchester coding technique are

arranged in a particular sequence. In this code bit '1' represents by high voltage which represents the half duration of a cycle and for the next half cycle an inverted signal will be send. In this format low voltage will send for the first half cycle when transmitting '0' and for the next half cycle a high voltage is send. There is a condition occur when it is difficult to define how many number of 1_S and Os in the data when sending a data having continuous high signals or continuous low signal (e.g.:111111110000000), Because there is no alteration from low to high or high to low for a particular time period. The only way to find it is to calculate the time duration of a signal but it is not reliable. So this condition can be avoided by using the coding technique in this paper Manchester and fm0 format are use. In Manchester format there will always be a transition from low to high or high to low for each bit. As a result by using Manchester coding the error probability becomes low and data received by the receiver is same as the code word and it becomes easier to detect data from channel for receiver.

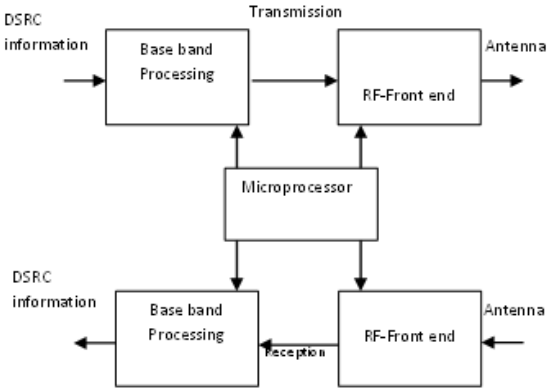

Fig 1: DSRC Transceiver

The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts are dedicated for transmission and receiving, respectively. This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end.

Literature Review

The VLSI architectures of FM0 and Manchester encoders are reviewed as follows Reference [1] proposed a fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encoding. The proposed method works on some parameters like TSMC, maximum operating frequency, Power consumption etc. Reference [2] glitch is introduced at the input of MUX−1 that causes logic-fault on coding. This problem is solved by using XNOR with the inverter. Reference [3, 4, 5, and 6] presents review on a review on Evaluation of various forms of DSRC system based on FMO/ Manchester encoding using SOLS technique and also compare this technique with other techniques. Reference [7, 8] proposed a fully reused VLSI architecture using SOL's technique for both FM0 and Manchester encodings. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. Reference [9] proposed a system to minimizing the problem of coding-diversity between FM0 and Manchester encodings that causes the limitation on hardware utilization of VLSI architecture design. This paper is realized in180nm technology with outstanding device efficiency. The power Consumption is 29392.843nW for Manchester encoding and FM0 encoding. Reference [10] proposed SOLS technique to overcome the problem of hardware utilization of VLSI design used for the DSRC dedicated short-range communication. The SOLS technique improves the hardware utilization rate from fifty seven.14% to 100% for each FM0 and Manchester encodings. Reference [11] proposed a method for power reduction in VLSI architecture using FM0 and Manchester encoding. The power consumed is 0.72 mw for Manchester encoding. The power consumption is 0.14 mw for FM0 encoding. Reference [12, 13, 14, 15] the paper presents coding diversity between FM0 and Manchester encodings that causes the limitation on hardware utilization of VLSI architecture design. The SOLS technique improves the Hardware Utilization Rate (HUR) from 57.14% to 100% for both FM0 and

Manchester encodings. Reference [16] presents Miller encoding which is integrated with FM0 and Manchester encoding architecture for the application of Dedicated Short Range Communication (DSRC). . This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works. In reference [17, 18] SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce the transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components.

Coding Principle of FM0 And Manchester Code

Coding principles of FM0 code and Manchester code is describe as follows.

For any coding scheme there is a need of Input data represented by X and a clock signal represented by C respectively. And with the help of some basic principle of such coding scheme the data be encoded decoded. Such that the principle of Manchester and FM0 coding scheme and such conditions are discussed below.. A. FM0 Encoding is shown in Fig. 2, for each X, the FM0 code consists of two parts: one for former-half cycle of CLK A and the other one for later-half cycle of CLK B. The coding principle of FM0 is listed as the following three rules.

1) If X is the logic-0, then there is a transition between A and B.
2) If X is the logic-1, no transition is acceptable between A and B.
3) The transition is achieved among each FM0 code no matter what the X is.

Example of FM0 coding is shown by Fig.2. Here the wave form is represented for the first cycle is such that X is logic-0; therefore, a transition occurs at the middle of the bit duration, according to rule 1. For simplicity, this transition is initially set from logic-0to1. According to rule 3, a transition is takes place at each end of the bit, and thereby the logic-1 is changed to logic-0 in the establishment of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the X of logic-1. Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

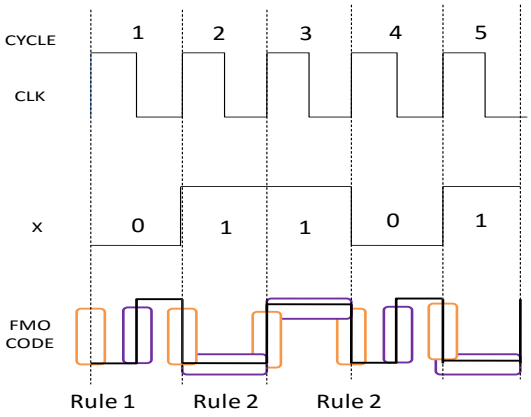

Fig 2: Example of FMO Encoding

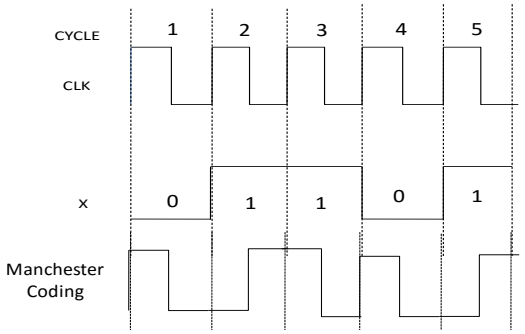

Fig 3: Example of Manchester Coding

` XOR operation is used to perform the basic principle of Manchester encoding between clock and input signal. Manchester encoder always changes its state between the centres of each cycle. The Manchester coding example is shown in Figure. 3.

Hardware Architecture of FM0 And Manchester Code

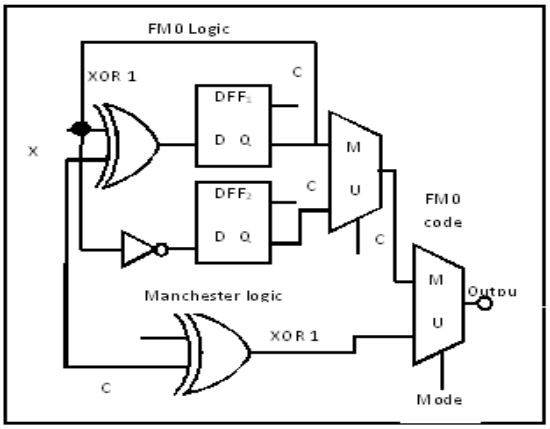

Fig 4: Hardware architecture of the fm0/Manchester code

Figure 4 represents the hardware architecture of proposed model. The upper part is denoted the fm0 code and then the bottom part are denoted as the Manchester code. In fm0 code the DFF1 and DFF2 are used to store the state code of the fm0 code and also mux_1 and not gate is used in the fm0 code. When Mode value is '0' fm0 code is work. When Mode value '1'is selected then it givs output as Manchester code and this code is develop only by XOR the data with the clock. The hardware utilization rate is defined as the following. The HUR rate is given below the following section

$$HUR = {}^{AC}/_{TC} * 100\ \%$$

AC- Active Components

TC- Total components

- Active components means the components are work in the both fm0 and Manchester code.
- The total components means the number of the components are present in the whole circuit.

Proposed SOLS Technique for FM0 and Manchester Design

(SOLS) similarity-oriented logic simplification technique improves the hardware utilization rate at some present for each FM0 and Manchester encodings. The SOLS technique is classified into two parts area compact retiming and balance logic operation sharing.1) in area compact retiming is shown by figure 5. Fm0 the state code of the each state is stored into two D flip flop DFF1and DFF2 .The Change in the state depends on state code that depends on the previous state of D flip-flop 1 i.e., 1(t-1) instead of the both the flip-flop. The previous state of both the flip-flop is denoted by 2(t-1) and 1(t-1) and 2(t), 1(t) represents the current state.

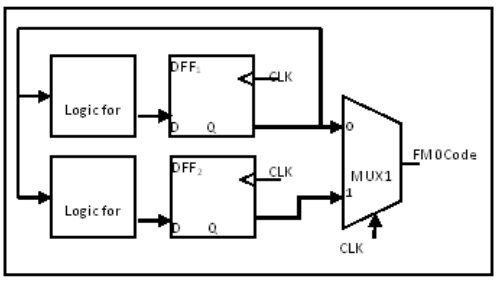

Fig 5: Area Compact Retiming

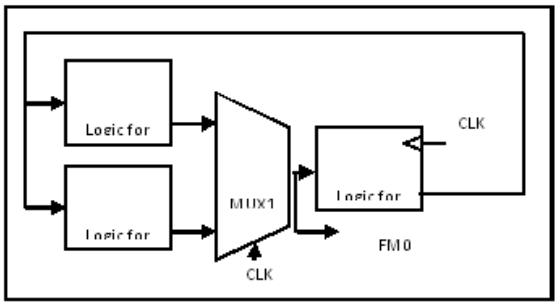

Fig 6: FM0 encoding without area compact retiming

To store the single bit output of the FM0 D-flip-flop is used that stores the previous state of the coding to generate the next one. As shown in figure 6 d flip-flop is used and the output of the fm0 depends on both the flip-flop it generates the output by comparing present data of both flip-flop 2(t) and 1(t).This is done to avoid the asynchronous faults. DFF1 is assumed to be positive-edge triggered flip flop shown in figure 6. At each cycle, the FM0 code, comprising 2 and 1, is derived from the logic of 2(t) and the logic of 1(t), respectively.

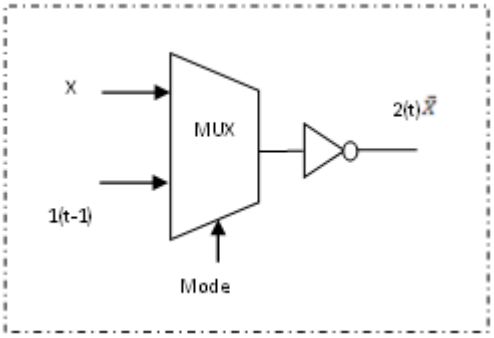

Fig 7: FM0 encoding with area compact retiming

By using the CLK signal in the MUX_1 the output of the flip-flop is switch between D flip-flop 1(t) and 2(t). The output of the DFF1 is directly updated from the logic of 1(t) with 1- cycle. When the CLK is logic-0, the output of DFF1 1(t) is given to the MUX−1.Then the upcoming positive-edge of CLK updates it to the Q of DFF

1. The timing diagram for the Q of DFF1 is consistent whether the DFF1 is relocated or not.
2. Balance logic operation shearing: XOR operation is used to generate the logic of Manchester encoding. The equation of the XOR gate is given below.

   X XOR CLK=X $\overline{CLK}$+$\bar{X}$ CLK

The concept of balance logic-operation sharing is to incorporate the X into both flip-flop output 2(t) and

1(t). MUX_2 decides the mode wether the output is taken from the fm0 or Manchester. Figure 8 represents the logic for balance logic sharing given the following.

Here, MUX Mode defines the Output is FM0/Manchester. If Mode is '0' that means the output is FM0 and if Mode is '1' then output is Manchester. The 2(t)/ $\bar{X}$can be derived from an inverter of 1(t − 1), and X. The logic for 2(t)/ $\bar{X}$ can share the same inverter, and then a multiplexer is placed before the inverter to switch he operands of 1(t − 1) and X. The Mode of the MUX indicates either FM0 or Manchester encoding. The similar concept can be also applied to the logic for 1(t)/X. Nevertheless, this architecture exhibits a drawback that the HUR of this architecture is limited because XOR is only dedicated to FM0 encoding, and is not shared with Manchester encoding. The X can be also interpreted as the X 0, and thereby the XOR operation can be shared with Manchester and FM0 encodings, where the multiplexer is not responsible to switch the operands of 1(t−1) and logic-0. This architecture shares the XOR for both 1(t) and X, and there by increases the HUR.

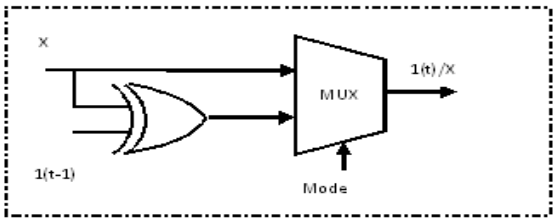

Fig 8: Balance logic operation sharing

Discussion of Results

The present design is simulated and synthesized using Xilinx ISE Tool. Fig-9 and Fig.10 show the Block Diagram and the RTL Schematic diagrams of FM0-Manchester Encoder design based on simulation. Fig.11 Represent the waveform simulation diagram of the encoder design.

Fig 9: Block diagram of FM0/Manchester Encoder

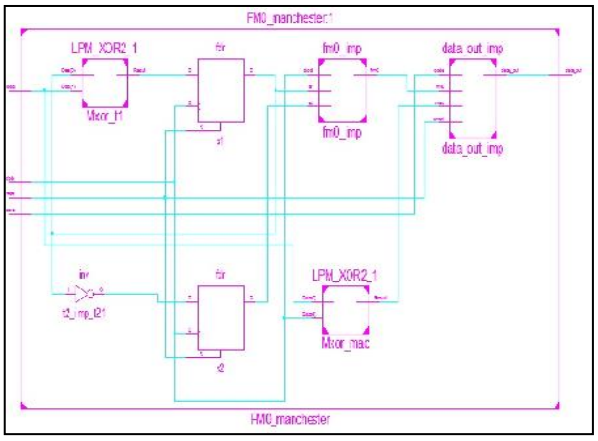

Fig10: RTL diagram of FM0/Manchester encoder

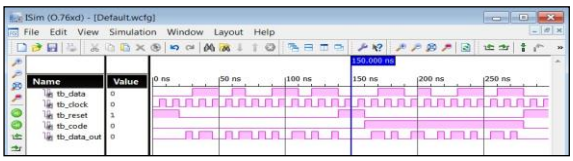

Fig 11: Represent the waveform simulation diagram of the encoder design

Xilinx Spartan3 FPGA is use to implement the encoder design. The hardware includes FPGA Kit, LCD 16x2 Display and Push-button board. Fig-12 shows the arrangement of the implementation kit setup and Fig-13 shows reset mode operation display on LCD.

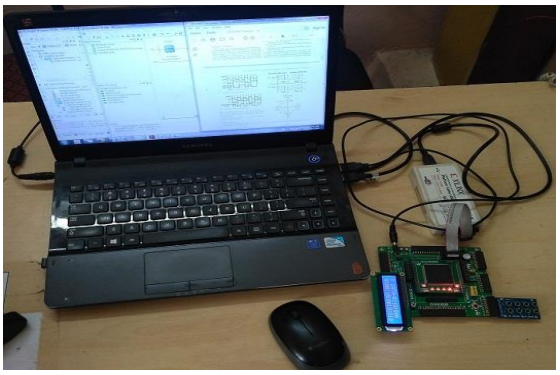

Fig.12: Hardware architecture of FM0/Manchester Encoder

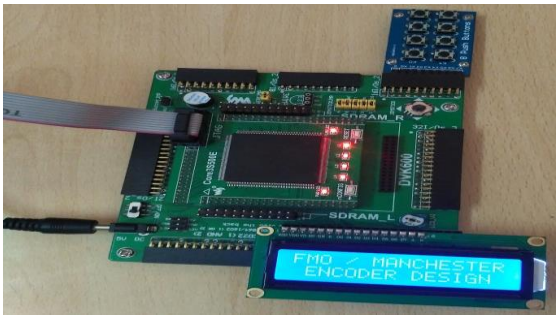

Fig.13: FM0-Manchester - Reset Mode Display

The hardware based design simulation is performed

on various input values. An example with input value "01101000" is shown for both FM0 and Manchester operational modes in Fig-14 and Fig-15 respectively.

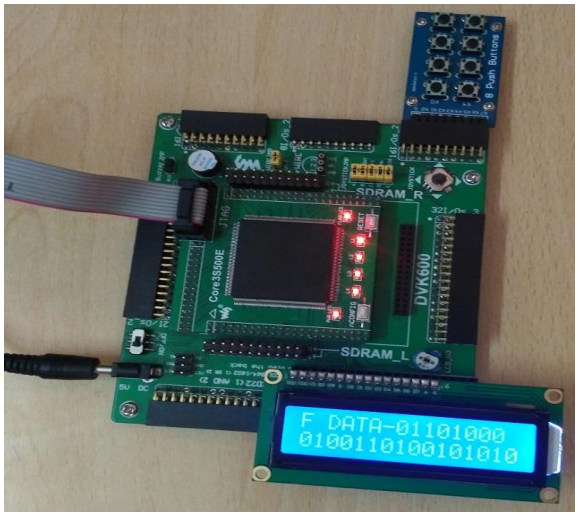

Fig 14: FM0 Input Example Display

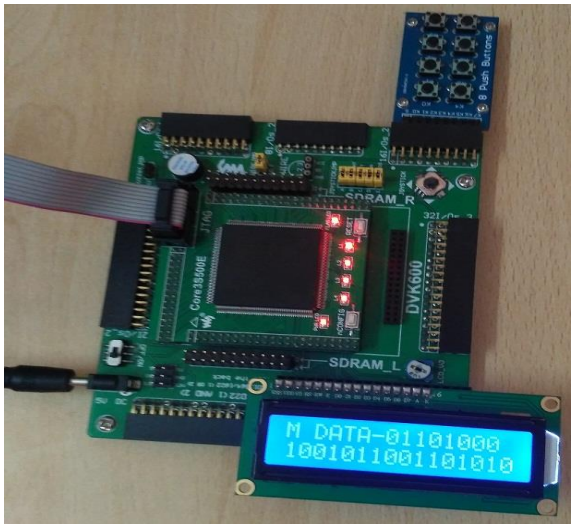

Fig 15: Manchester Input Example Display

The FPGA based hardware utilization summary of the implemented Encoder design is presented in Table-I and Table-II respectively. The hardware utilization is presented for software simulation based design and hardware implementation design.

TABLE I: Hardware Utilization of FM0/Manchester Encoder (Software Design Simulation Encoder)

Spartan-3E XC3S500E-4PQ208	**Total**	**FM0-Manchester Encoder**	
		Used	**%**
Slices	4656	2	0
Flipflops	9312	2	0
LUTs 4-Inputs	9312	4	0
Bonded IOBs	158	5	3

TABLE II: Hardware Utilization of FM0/Manchester Encoder (Software Design Simulation Encoder)

Spartan-3E XC3S500E-4PQ208	**Total**	**FM0-Manchester Decoder**	
		Used	**%**
Slices	4656	299	6
Flipflops	9312	244	2
LUTs 4-Inputs	9312	441	4
Bonded IOBs	158	23	14

These tables give the utilization of the hardware resources of the design in terms of flip-flops and slices. The flip-flops represent the sequential logic components required by the design for logic representation. The slice is a combination of Look-Up-Tables (LUT) and Flip-flops. Different LUTs are present in a FPGA. A LUT is a combination of combinational and/or sequential logic hardware that can be programmed to generate a specific output as per the requirement of design. A comparative analysis of the hardware utilization of the design in the present work with some of the existing works is presented in Table-III.

TABLE III: Comparative analysis of design based on hardware utilization

Reference	**Present Work**	**[19]**	**[15]**	**[19]**
Device	Xilinx FPGA Spartan 3	Xilinx FPGA Spartan 2	Xilinx FPGA	Xilinx FPGA Spartan2
Slices	2	5	2	1
Flipflops	1	4	2	2
LUTs 4-Inputs	3	10	3	2
Bonded IOBs	5	4	5	3

Conclusion

The limitation on VLSI architecture designing causes due to the coding-diversity between FM0 and Manchester encodings. The limitation analysis of FM0 and Manchester encodings is discussed in detail. Hence, the fully reused VLSI architecture using SOLS (Similarity

oriented logic simplification) technique for both FM0 and Manchester encodings is modified. The SOLS technique eliminates the limitation by two core techniques: area-compact retiming and balance logic-operation sharing. Area-compact retiming relocates the logic elements effectively. The Balance Logic operation sharing technique combines FM0 and Manchester encodings to produce balanced computation time. Results show the improved hardware utilization rate through which power consumption is reduced. This project not only develops VLSI architecture for FM0 and Manchester Encoding but also improves the performance of both encoding schemes.

References

[1] Yu-Hsuan Lee, and Cheng-Wei Pan, "Fully Reused VLSI Architecture of FM0 and Manchester Encoding using SOLS Technique for DSRC Applications", IEEE Transaction on Very Large Scale Integration system Vol.23, NO.1, pp.19-29 January2015.

[2] S.P.Ramekar, and Dr.P.N.Chatur, "A Review on Fully Utilized Architecture for FM0, Manchester and Miller Encoding Using SOLS Technique", International Journal of Innovative Research in Computer and Communication Engineering, Vol. 4, Issue 2, pp.2517-2523 February 2016.

[3] Lalitha V, and Kathiravan S, "A Review of Manchester, Miller, and FM0 Encoding Techniques", Smart Computing Review, vol. 4, no. 6, pp.481-490 December 2014.

[4] Bhavik Mehta, and Prof. Munmun ghosal, "Review on FM0Manchester encoder-decoder used in DSRC based Applications", International Journal on Recent and Innovation Trends in Computing and Communication, Vol. 4 Issue. 4, pp.532-535, April 2016.

[5] Supriya S. Garade, and P. R. Badadapure, "Review of Fully Reused VLSI Architecture of Channel Encoding Using SOLS Technique for DSRC Applications", International Journal of Science and Research (IJSR), Volume 5 Issue 4, pp.2313-2315April 2016.

[6] M. Abinaya, and T. Suganya Thevi, "Evaluation of Various Forms of DSRC System- A Review", International Journal of Engineering Science Research Technology, November, 2014.

[7] T Sravan Kumar, and A. Madhukar Babu, "FM0/Manchester Encoding for DSRC Applications Using SOLS Technique", Journal Research in Electrical Electronics and communication, Vol.3, Issue 6.

[8] Ms. Jomcy Rani Xavier **,** and *Dr*. U. A.Kshirsagar, "Fully Reconfigured VLSI architecture of FM0, Manchester and Miller", International Journal of Engineering Research and General Science Volume 4, Issue 2,pp.839-846 March- April, 2016.

[9] T.Rajini, and G.Sataya Prabha, "Fully Rrused VLSI Architecture Of FM0/Manchester Encoding Using SOLS Technique For DSRC Application", International Journal of Research In Advance Engineering Technologies, Volume 5, Issue 1, pp.33-40, SEP 2015.

[10] S.Shaik Hussain, H.Somashekar, and D.V.Srihari Babu, "R10-Design and Realization of FMO/Manchester Encoding for DSRC Application Using SOLS Technique", International Journal of Advanced Research in Education Technology, Vol. 2, Issue 3, pp.81-84 (July - Sept. 2015).

[11] S.M.Subramanian, N.Nagaraj, R.Ajin, and J.Rasathi, "R11-Power Reduction in the VLSI Architecture of FM0 and Manchester Encoding" - International Journal for Scientific Research & Development| Vol. 2, Issue 12,pp.861-864 2015.

[12] V. Hemalatha, and P. Srividhya, "R12-Fully Reused VLSI Architecture of Miller Encoding using SOLS Technique for DSRC", International Journal of Advance Engineering and Global Technology, Vol.4, issue 1, pp.1718-1724, January 2016.

[13] Mohan R, Karthikkeyan A R, "Fully Reused VLSI Architecture for DSRC Applications Using SOLS Technique", International journal of engineering studies and technical approach,Vol.02, No. 4, pp. 137-149 April 2016.

[14] G.Keerthana, and Mrs.M.Bhuvaneswari, "R14-Design of an Efficient Encoder for DSRC Application Using SOLS Technique" International Journal of Advanced Research In

Management, architecture, Technology & Engineering, 2016.

[15] Arya Krishnan, and Anusree L. S., "R15-Reusable SOLS Encoder for DSRC Applications", International Journal of Science and Research (IJSR), Volume 4 Issue 2, pp. 1874-1878 February 2015.

[16] A.Syed Musthaba, and J.Sathya, "Fm0ManchesterMiller Encoding for Intelligent DSRC Transportation System", IOSR Journal of Electronics and Communication Engineering, PP.172-175, February 2015.

[17] K.Srinath, and V.Prasad, "Design and Implementation of DSRC Encoders for Efficient Hardware Utilization" International Journal of Innovative Research in Science, Engineering and Technology, Vol. 4, Issue 7, pp.5132-5142, July 2015.

[18] Mr.S.PRakash, K.Umadevi, and Dr.V.Nagarajan, "Area Efficient Encoding Technique for Reducing Power In DSRC" International Journal of Innovative Research in Information Security, Volume 1, Issue 3 ,pp.7-12 September 2014.