International Journal of Engineering Research-Online
A Peer Reviewed International Journal
Articles available online http://www.ijoer.in; editorijoer@gmail.com

Vol.4., Issue.6., 2016
Nov-Dec.

RESEARCH ARTICLE

ISSN: 2321-7758

OPTIMIZATION OF LEAKAGE POWER AND INRUSH CURRENT IN MTCMOS DESIGNS USING WAKE UP CONTROL TECHNIQUE

G.MANIKANNAN[1], P. PRABAKARAN[2], M. SELVAGANAPATHY[3]

[1,2,3]Assistant Professor, ECE

CKCET, Cuddalore, Tamilnadu

G. MANIKANNAN

M. SELVAGANAPATHY

P. PRABAKARAN

ABSTRACT

Power gating is effective for reducing standby leakage power as multi-threshold CMOS (MTCMOS) designs have become popular in the industry. However, a large inrush current and dynamic IR drop may occur when a circuit domain is powered up with MTCMOS switches. This could in turn lead to improper circuit operation. Hence we propose a new power-gating technique that is tolerant to process variations and scalable to more than two intermediate power-off modes. The proposed design requires less design effort and offers greater reduction in leakage power. We also propose a configurable domino-delay circuit for implementing the sequence. In addition, it can be combined with existing techniques to offer further static power reduction benefits. Analysis and extensive simulation results of RCA demonstrate the effectiveness of the proposed design.

Keywords: Dynamic IR, inrush current, multi-threshold CMOS (MTCMOS), power gating, Leakage power, multi-mode power switches, process variation, reconfigurable power-gating structure.

I. INTRODUCTION

Energy efficiency is important to battery-powered portable devices such as smart phones, GPS, PDAs, and tablets. However, the leakage current of these devices has increased significantly with the shrinking of semiconductor process technologies. The most straightforward and effective method for reducing standby leakage is power-gating, which cuts off the power supply (or ground) to a power-gated domain when it is in an idle state and resumes the power supply when it is in an active state. In this paper, we attempt to manage the switching transients generated by digital CMOS gates by localizing them in the same region of their origin [9], thus preventing them from coupling to other analog systems on the same substrate.

The multi-threshold CMOS (MTCMOS) technique [1] employs high- transistors to implement always-on circuits, such as power switches, retention flip-flops, and always-on buffers, to minimize their leakage power consumption. Dynamic power is tackled nowadays by the reduction of the supply voltage level.

Dynamic energy is proportional to the square of the supply voltage. Thus, a lower voltage level yields a quadratic reduction in the energy consumption. To further reduce the dynamic power, systems-on-chip (SoCs) are partitioned into voltage islands with separate supply rail and unique power characteristics [2]–[4].

After the power switches are allocated, the sequence that turns on the power switches for a domain (called the power-up sequence) determines the voltage ramp-up time and the inrush current of the domain. Moreover, as devices keep shrinking, the channel length shortens and the gate oxide thickness reduces, increasing the gate-induced drain leakage, the gate oxide tunneling current, and the junction leakage [5]. For technologies below 90 nm, leakage (static) power is so high that it is comparable in magnitude to dynamic power consumption.

Many techniques have been presented in the literature for reducing static power. One common approach is to synthesize the circuit using dual-Vt libraries [6]. High-Vt cells reduce the leakage current at the expense of reduced performance; thus their use on noncritical circuit domains reduces the leakage power considerably without affecting circuit performance. Another technique exploits the fact that the leakage power consumed by each gate strongly depends on the input vector applied at the gate. Therefore, in order to reduce static power, it controls the input vector and the internal state of the circuit during periods of inactivity [7]–[11].

Fig. 1 illustrates a design tradeoff between the inrush current and the ramp-up time. The dotted line "A" indicates that all power switches are turned on simultaneously, thus, the current peaks very early and the virtual rail voltage reaches the VDD level quite early. The dashed line "B" interspersed with single dot represents a single chain fabric, where the peak current is intrinsically small as power switches are turned on one by one per100 ps in a sequential fashion. However, the inrush current may still exceed the specified constraint. Turning on power switches sequentially with larger time interval (e.g., 200 ps) can reduce the inrush current at the expense of increased area and ramp-up time (dashed line "C"). This study proposes a framework to schedule the power-up sequence of the power switches. This approach minimizes power ramp-up time while limiting the inrush current (solid line "D" in Fig. 1). In this framework, the power-up sequence turns on one bank of power switches at a time, and employs a configurable delay circuitry to control the activation of the next bank. We also propose a new model for estimating inrush current for very large-scale MTCMOS designs.

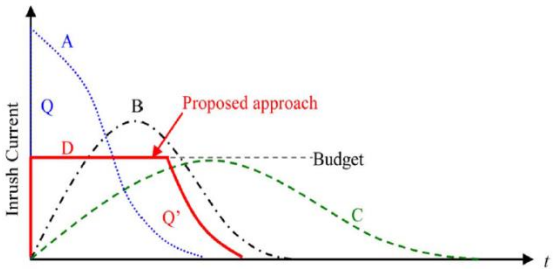


Fig.1. Tradeoff of inrush current and the expected current budget control.

During power-up, a power switch (PSW) behaves like a current source and remains in the saturation region for a while. The power-gated devices connected to the virtual rail VDDV behave like resistors until the virtual rail is charged to the normal operating voltage. As depicted in Fig. 3, we model a power switch as a voltage-dependent current source (i1, i2,….in) and a gate (U1, U2,….Un) including wires as a lumped resistance and a lumped capacitance Ceff. T1, T2,…., Tn denote the times at which the associated power switch can be turned on.

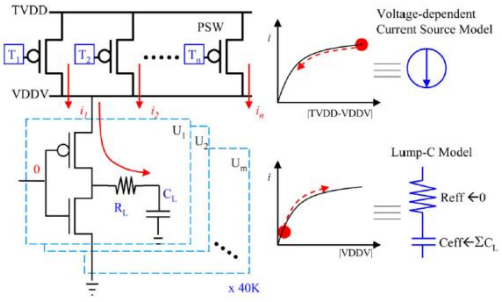


Fig.2. Power ramp-up and effective capacitance modeling.

II. MULTI-MODE POWER-GATING ARCHITECTURE

Fig. 2 presents the proposed design. It consists of the main power switch transistor MP and two small transistors M0 and M1, each corresponding to an intermediate power-off mode (M0 corresponds to the dream mode and M1 corresponds to the sleep mode). Transistor MP is a high-Vt transistor and it remains on only during the active mode. Transistors M0 and M1 are small low-Vt transistors that are turned on only during the corresponding power-off mode. (i.e., M0 is turned on during the dream mode and M1 is turned on during the sleep mode). The various modes of operation are as follows.

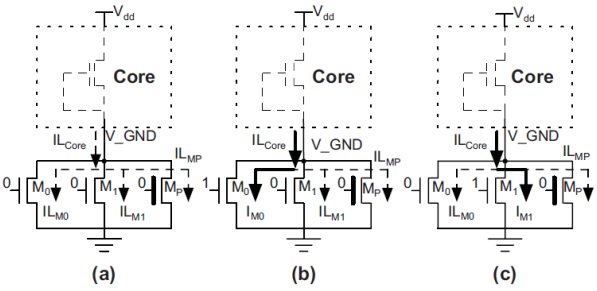


Fig.3. Proposed architecture: (a) snore mode, (b) dream mode, (c) sleep mode.

The various modes of operation are as follows.

1) Active Mode: Transistors MP, M0, M1 are on.
2) Snore Mode: Transistors MP , M0, and M1 are off as shown in Fig. 2(a). In this case, the leakage current ofthe core, I Lcore, is equal to the aggregate leakage current flowing through transistors M0, M1, MP (I Lcore = I LM0 + I LM1 + I LMP), which is very small (note that M0, M1 are small transistors and MP is a high- Vt transistor). Thus the voltage level at V_GND is close to Vdd and the circuit consumes a negligible amount of energy, but the wake-up time is high.
3) Dream Mode: Transistor M0 is on and transistors MP and M1 are off as shown in Fig. 2(b). In this case, the current flowing through transistor M_0 (and thus the aggregate current flowing through M0, M1, and MP) increases because M0 is on (IM0 > I LM0). The exact value of IM0 depends on the size of transistor M0, and it sets the virtual ground node at a voltage level which is lower than Vdd (i.e., VV_GND < Vdd). Thus the static power consumed by the core is higher compared to the snore mode, but the wake-up time is less.
4) Sleep Mode: Transistor M1 is on, and MP, M0 are off as shown in Fig. 2(c). Provided that transistor M1 has larger aspect ratio than M0 (WM1/LM1 > WM0/LM0), the aggregate current flowing through M0, M1, and MP increases even more when M1 is on (note that IM1 > IM0). Consequently, the voltage level at the virtual ground node is further reduced compared to the dream mode and thus the wake-up time decreases at the expense of increased power consumption.

III. RIPPLE CARRY ADDER

A full adder is a combinational circuit that performs the arithmetic sum of three input bits: augends Ai, addend Bi and carry in in C from the previous adder as in fig.4. Its results contain the sum Si and the carry out, out C to the next stage. So to design a 4-bit adder circuit we start by designing the 1 –bit full adder then connecting the four 1-bit full adders to get the 4-bit adder as shown in the diagram above. For the 1-bit full adder, the design begins by drawing the Truth Table for the three input and the corresponding output SUM and CARRY. The Boolean Expression describing the binary adder circuit is then deduced. The binary full adder is a three input combinational circuit which satisfies the truth table below.

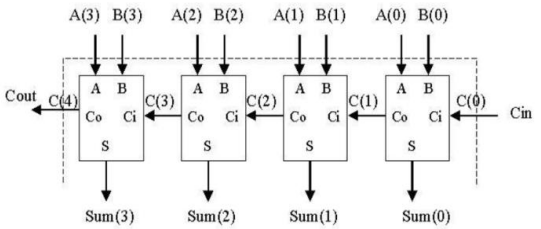
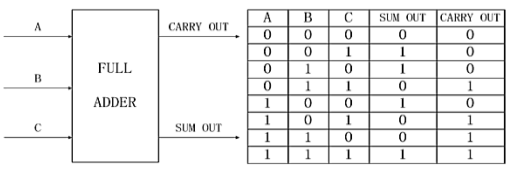


Fig.4. 4 Bit Adder



A	B	C	SUM OUT	CARRY OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig.5. Symbol and Truth Table of Full Adder

In fig.5. shows the symbol and truth table of full adder and fig.6. shows the gate level diagram of full adder.

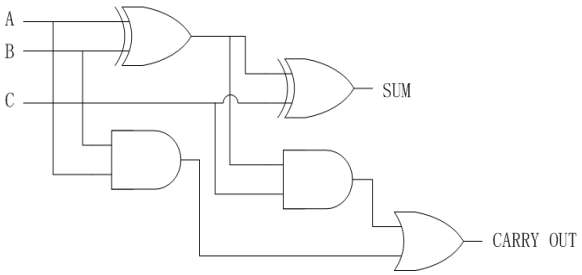


Fig.6. Gate level Diagram of Full Adder

To design a 4-bit adder now we cascade 4 1-bit adders as shown in Fig.7.

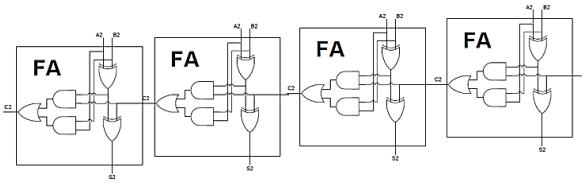


Fig.7. 4-bit Ripple Carry adder

IV. SIMULATION RESULTS

To analyse the Ripple Carry Adder with and without MTCMOS in different modes (Active and Dream) and its leakage power is calculated. The circuit is designed using Cadence@Virtuoso tool by GPDK foundry in 0.18µm technology. For this analysis a single bit adder (Fig.8.) is cascaded for four single bit adder (Fig.9.).

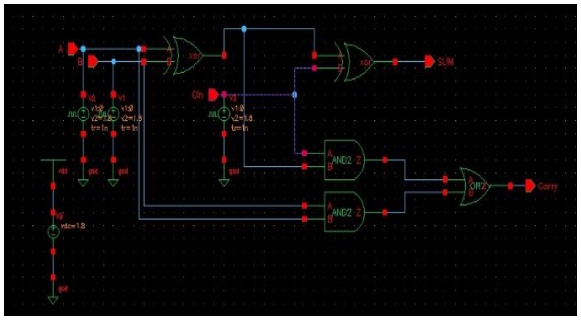


Fig.8. Schematic of Full Adder using Cadence

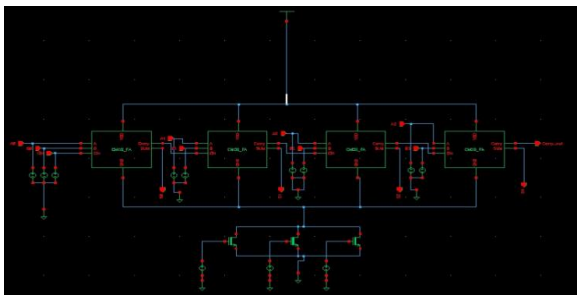


Fig.9. Schematic of 4-Bit Adder using Cadence

In this fig.8. 4-Bit Ripple Carry Adder is designed and it is connected with the MTCMOS at the NMOS with ground end. The Vdd is connected without any MTCMOS at the top end.

TABLE I: LEAKAGE POWER WITH NMOS ONLY

LEAKAGE POWER	
DREAM MODE	0.002189978581532051
ACTIVE MODE	0.003884902704680259

In the designed fig.9., the leakage power of dream mode and active mode is calculated for NMOS alone and is resulted in the table II.

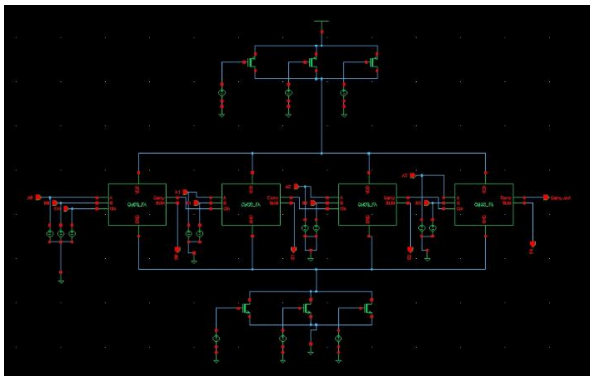


Fig.10. Schematic of 4-Bit Adder using Cadence with MTCMOS

In this fig.10. 4-Bit Ripple Carry Adder is designed and it is connected with the MTCMOS at the NMOS with ground end and Vdd is connected with PMOS at the top end.

TABLE II: LEAKAGE POWER WITH BOTH NMOS AND PMOS

LEAKAGE POWER	
DREAM MODE	0.002189978581542283
ACTIVE MODE	0.003884902704802092

In the designed fig.9., the leakage power of dream mode and active mode is calculated for NMOS alone and is resulted in the table II.

TABLE III: LEAKAGE POWER AT DIFFERENT CONDITION

LEAKAGE POWER	
PMOS ON	$3.619894544273368e^{-11}$
NMOS ON	0.00141190673370357
BOTH OFF	$3.620108360802192e^{-11}$

The leakage power can be calculated at different condition. In table III the power for PMOS alone ON, NMOS alone ON and both NMOS and PMOS in OFF condition.

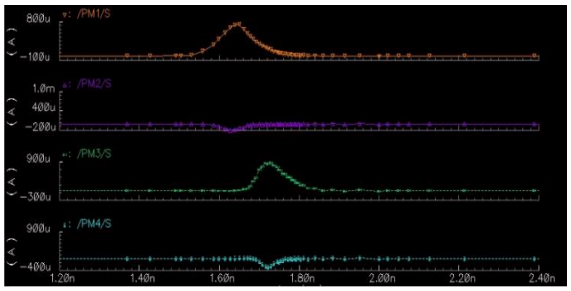


Fig.11. Inrush current at different nodes

In this fig.11. the graph shown is the inrush current variation at different nodes of the circuit such as PM1, PM2, PM3 and PM4. Further the concept can be implemented in different circuits such as 8-bit adder, flip-flop, comparator, etc., and their leakage power and inrush current values can be noted and compared for the better results. The circuit can be designed at 90nm sizing with the same results without any degrading in the performance.

V. CONCLUSION

The simulation results from the circuit design shows that the use of MTCMOS as PMOS and NMOS at both GND and VDD end highly reduces the leakage power of the circuit. This can be further improved by sequential buffer in turn it reduces the inrush current produce at the nodes. Thus by reducing both inrush current and leakage power, device damage can be reduced and results with better efficiency rate obtained for circuit design.

REFERENCES

[1]. S.Mutoh, T. Douseki, Y. Matsuya, T. Aoki, and J. Yamada, "1 V highspeed digital circuit technology with 0.5 m multi-threshold CMOS," in *Proc. IEEE 6th Int. Annu. ASIC Conf.*, 1993, pp. 186–189.

[2]. C. Long and L. He, "Distributed sleep transistors network for power reduction," in *Proc. DAC*, 2003, pp. 181–186.

[3]. M. Anis, S. Areibi, M. Mahmoud, and M. Elmasry, "Dynamic and leakage power reduction in MTCMOS circuits using an automated efficient gate clustering technique," in *Proc. DAC*, 2002, pp. 480–485.

[4]. S. H. Chen and J. Y. Lin, "Experiences of low power design implementation and verification," in *Proc. ASP-DAC*, 2008, pp. 742–747.

[5]. J. Kao, S. Narendra, and A. Chandrakasan, "MTCMOS hierarchical sizing based on mutual exclusive discharge patterns," in *Proc. DAC*,1998, pp. 495–500.

[6]. C. Hwang, C. Kang, and M. Pedram, "Gate sizing and replication to minimize the effects of virtual ground parasitic resistances in MTCMOS designs," in *Proc. ISQED*, 2006, pp. 741–746.

[7]. J. Kao, A. Chandrakasan, and D. Antoniadis, "Transistor sizing issues and tool for multi-threshold CMOS technology," in *Proc. DAC*, 1997,pp. 409–414.

[8]. A. Davoodi and A. Srivastava, "Wake-up protocols for controlling current surges in MTCMOS-based technology," in *Proc. ASP-DAC*, 2005,pp. 868–871.

[9]. A. Ramalingam, A. Devgan, and D. Z. Pan, "Wake-up scheduling in MTCMOS circuits using successive relaxation to minimize ground bounce," *J. Low Power Electron*, vol. 3, no. 1, pp. 28–35, Apr. 2007.

[10]. Y. T. Chen, D. C. Juan, M. C. Lee, and S. C. Chang, "An efficient wake-up schedule during power mode transition considering spurious glitches phenomenon," in *Proc. ICCAD*, 2007, pp. 779–782.

[11]. H. Jiang and M. Marek-Sadowska, "Power gating scheduling for power/ground noise reduction," in *Proc. DAC*, 2008, pp. 980–985.

[12]. Zhaobo Zhang, Xrysovalantis Kavousianos, Krishnendu Chakrabarty, and Yiorgos Tsiatouhas. " Static Power Reduction Using Variation-Tolerant and Reconfigurable Multi-Mode Power Switches" in Proc. IEEE VLSI Systems 2008.

ABOUT THE AUTHORS

Mr. G. Manikannan has received his M.E in Electronics and Communication Engineering and B.E – Electronics and Communication Engineering from Anna University, Chennai. Research areas are Low Power IC Design, Digital & Analog Circuits, VLSI Design etc. Currently working as Assistant Professor, Department of ECE, CK College of

Engineering & Technology, Cuddalore District, Tamilnadu.

Mr. M. Selvaganapathy is currently pursuing his Ph.D in Image Processing from Annamalai University, Chidambaram. He has received his M.E in Communication Systems and B.E – Electronics and Communication Engineering from Anna University, Chennai. His research areas are Digital Image Processing, Wireless Networks, Embedded Systems and automations, process control and applications, etc.

Mr. P. Prabakaran has received his M.E in Optical Communication from Anna University, Trichy and B.E – Electronics and Communication Engineering from Anna University, Chennai. His research areas are Digital Image Processing, Digital Signal Processing, Optical Communication and Networks, etc.