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RESEARCH ARTICLE

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A DOUBLE ENDED WRITE SINGLE ENDED READ DECOUPLED 9T SRAM CELL WITH FASTER READ SPEED AND IMPROVED READ STABILITY

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ABSTRACT

In this paper a double ended write single ended read decoupled SRAM cell is proposed. Design metrics of the proposed cell are examined and compared with conventional 6T, 7T and 9T SRAM Cell. Proposed SRAM cell offer improvement during read operation in terms of speed. It offers 79.06% shorter read delay and 59.8% shorter leakage power. The proposed cell also shows improvement in read stability. It offers 5.45x higher RSNM (read static noise margin) at 1V compared to conventional 6T SRAM Cell at 32nm.

Keywords—CMOS; SRAM; single ended; Read Delay; Read Stability; Leakage power.

1. INTRODUCTION

This paper is to introduce a high speed single ended Read decouple 9T SRAM Cell with improved stability as compare to other conventional cells. SRAM uses bi-stable latching circuitry made of Transistors/MOSFETS to store each bit. Compared to Dynamic Random access memory (DRAM), SRAM doesn't have a capacitor to store the data, hence SRAM works without refreshing[1]. In SRAM the data is lost when the memory is not electrically powered. Advances in chip design using CMOS technology have made possible the design of chips for higher integration, faster performance, and lower power consumption. To achieve these objectives, the feature size of CMOS devices has been dramatically scaled to smaller dimensions over the last few years. Power consumption of SRAMs account for a significant portion of the overall chip power consumption and due to high density, low power operation is a feature that has become a necessity in today's microprocessors. Hence, power consumption of SRAM modules must be reduced and has been under extensive investigation in the technical literature.

SNM is the important parameter for stability analysis of SRAM Cells. SNM affects both read margin and write margin, which is related to the threshold voltages of the NMOS and PMOS devices in SRAM cells. Typically, to increase the SNM, the threshold voltages of the NMOS and PMOS devices need to be increased[2]. There are two purposes of an SRAM design: First is to provide a direct interface with the CPU at speeds not attainable by DRAMs and second is to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. The second driving force for SRAM technology is low power applications. In this case,

SRAM are used in most portable equipment because the DRAM refresh current is several orders of magnitude more than the low-power SRAM standby current[3]. To increase the read speed of the cell read delay of the cell should be low this can be done by increasing the read current. As read current increase, the read delay will decrease.

2. Related works

(a)Conventional 6T SRAM Cell- Figure 1 shows the schematic of a conventional 6T SRAM cell in which two back to back inverters are used to provide a positive feedback loop to hold the data. Two access transistors are also used to enable read and write operations. The 6T cell is widely used and accepted as the standard SRAM structure.

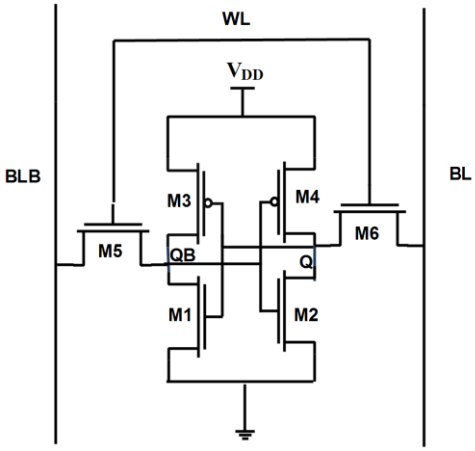

Figure 1. The schematic of conventional 6T SRAM Cell

Due to severe increase in threshold voltage (*V*t) fluctuation caused by global and local process variations in ultra-short-channel devices, 6T SRAM cell and its variants cannot be operated at further scaled supply voltages without parametric and functional failure causing yield loss. Low power 6T SRAM cell could reduce access delay and write power but not to the extent level[4]. In conventional 6T cell, the read operation is quite a slow process, due to undesirable time the access transistors takes for activation to access the latch.

(b) 7T SRAM Cell- In 7T SRAM cell structure an additional transistor placed in the ground path of a 6T SRAM cell to reduce leakage while the cell is in standby mode. In the standby mode, the bottom transistor is intended to cut-off the ground path and to eliminate the leakage paths through the inverter transistor sources but this cell cannot increase the read speed[5].

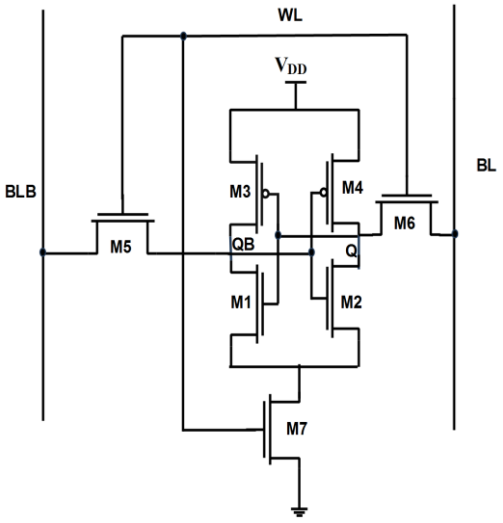

Figure 2. The schematic of 7T SRAM Cell

(c) 9T SRAM Cell- A novel 9T SRAM cell with enhanced data stability and reduced leakage power consumption is shown in Figure 3. The upper sub-circuit of the new memory cell is essentially a 6T SRAM cell with minimum sized transistors. The two write access transistors (M5 and M6) are controlled by a write signal (WR). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (M7 and M8) and the read access transistor (M9). The operations of M7 and M8 are controlled by the data stored in the cell. M9 is controlled by a separate read signal (RD)[6].

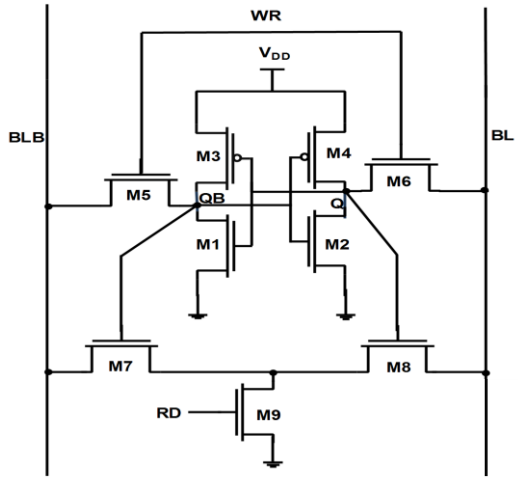

Figure 3. The schematic of 9T SRAM Cell

(d)Proposed 9T SRAM Cell- The SRAM structures have been designed to limit the noise in read operation by adding a Read de-couple circuit for read operation which isolates the basic memory element from the external noise keeping the access transistors disabled while reading the cell. In the designing of proposed cell three more transistor is used as compared to conventional 6T SRAM cell. It consist single ended read and double ended write operation. Read operation is controlled by the control signal RD and $\overline{RD}$ while write operation is controlled by WR signal. Transistor M8 and M9 form a transmission gate connected to RBL as shown in figure 4.

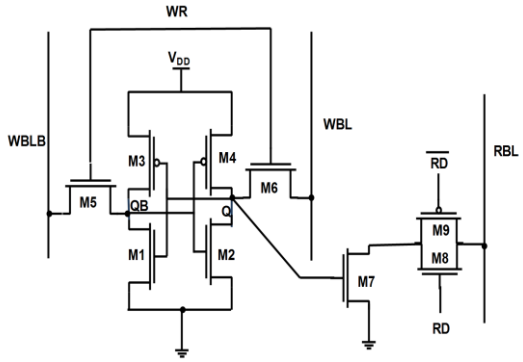

Figure 4. The schematic of proposed 9T SRAM Cell

Read operation- The aim of the read operation is to successfully retrieve the data stored on the inverter pair without causing any unwanted flipping of the data. let us assume that logic "1" is stored at node Q. The read bit line (RBL) is precharged to a value as close to V_{DD} as possible. The read operation is started by asserting the control signal RD, enabling pass transistor M7 and transmission gate (M8, M9). For a correct read operation, the values stored at Q is connected to the gate terminal of transistor M7,which make it on and read operation can be done by discharging the RBL through M8-M9-M7.

Write operation- The aim of the write operation is to flip the data stored on the inverter pair. The write bit line WBL is forced to logic "0" level by the write circuitry while WBLB remains at the precharged level. As the access transistors are turned on by asserting the write control signal WR, the node voltage of QB remains below the threshold voltage of M3 transistor. However, the writing occurs on the WBL side where the voltage at node Q starts to drop from the original logic "1" level. Once this voltage reaches a value less than the threshold voltage of M1, the second inverter gets activated and as a result of positive feedback, the logic levels on the nodes Q and QB get flipped.

Hold operation- In hold state both the write control signal (WR) and read control signal (RD) are disabled so the access transistors are in off state so there is no conduction take place to discharge the Q and QB node and data remain same.

3. Simulation and Result- Figure 5 shows the simulated wave form of read write and hold operation of proposed 9T SRAM Cell by using HSPICE tool at 32nm technology node.

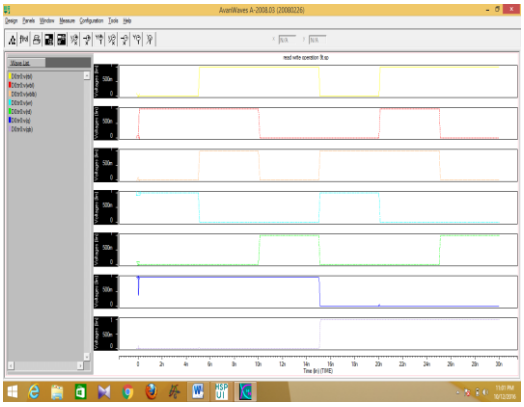

Figure 5. Simulated waveform of read, write and hold operation of proposed 9T SRAM Cell.

(a) Estimation of Read Delay- Read delay is calculated as the time taken to discharge the read bit line (RBL) by 50 mV from its initial high value after the read control signal (RD) starts to increase from its initial low value (i.*e.*50% of full swing)[7].

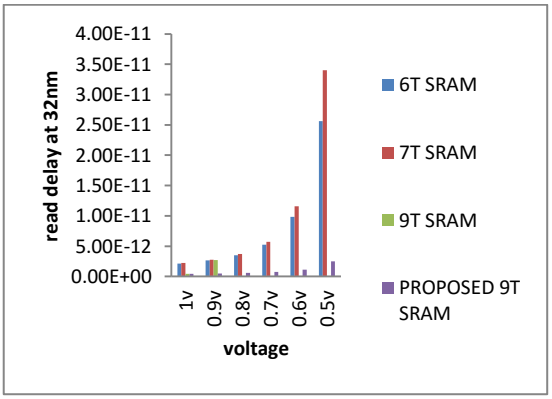

Figure 6. Read delay comparison of different SRAM Cells at 32 nm technology node.

Above figure shows read delay comparison between different SRAM Cells. Sense amplifier failed to find the Read delay of 9t SRAM Cell below 0.9v supply voltage. It is clear from above graph that read delay of proposed 9T SRAM Cell is less as compared to other conventional cells.

(b) Static Noise Margin- The stability of SRAM circuits depends on the static noise margin. There are two methods to measure the SNM of SRAM cell. First method is a graphical approach in which SNM can be obtained by drawing and mirroring the inverter characteristics and then finding the maximum possible square between them. Figure 7 shows the standard setup of SNM.

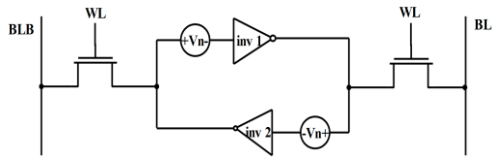

Figure 7. The standard setup for SNM definition of conventional 6T SRAM Cell.

The second approach involves the use of noise source voltages at the nodes. In a graphical technique, Plot the Voltage Transfer Characteristic (VTC) of Inverter 2 (inv2) and inverse VTC 1 from Inverter 1 (inv1). The resulting two lobed curves are called a "butterfly curve" and are used to determine the SNM. The SNM is defined as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve[8].

Read Stability Analysis- Read stability is analyzed by the estimation of read static noise margin (RSNM). RSNM is defined as the minimum noise voltage that can cause flipping the cell content of the storage nodes. It is considered that SRAM cell is most susceptible to noise during read operation. RSNM is estimated from the butterfly curve (as shown in Fig. 8) which is the VTCs (voltage transfer characteristics) during read operation.

The length of the maximum diagonal inside the butterfly curve is found 0.3708.

We have done the SNM calculation by this way with respect to above butterfly curve:

SNM = Maximum Side of the square inside the butterfly curve.

Maximum side of the Square = Maximum lengths of diagonal of Square / √ 2.

So, SNM = Maximum length of diagonal of square / √ 2.

SNM = 0.3708/ √ 2 = 0.262V at 1v power supply.

The Read Noise Margin of the proposed 9T SRAM Cell is same as the SNM of conventional 6T SRAM Cell in standby mode, because read operation is done through RBL Line by de-couple circuit. It is also same as the Read Noise Margin of conventional 9T SRAM Cell.

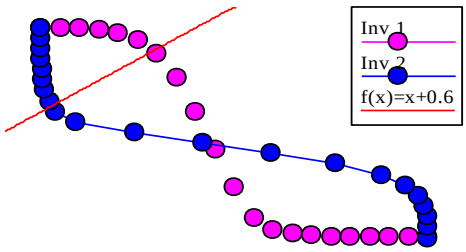

Figure 8. Butterfly Curve for Read Noise Margin of proposed 9T SRAM Cell.

TABLE 1-READ NOISE MARGIN OF DIFFERENT SRAM CELLS

SRAM CELL	RNM (V)
6T SRAM	0.048
7T SRAM	0.011
9T SRAM	0.262
Proposed 9T SRAM	0.262

Write Ability Analysis- Write ability is analyzed by estimation of write static noise margin (WSNM). WSNM is used to investigate the ability of an SRAM cell to pull up the node voltage, which is initially storing "0" beyond the threshold voltage of the inverter, which is initially storing "1", so that cell content of the storage nodes can flip successfully. WSNM is estimated as a side length of the smallest square that can be embedded inside the lower half of the read and write VTCs (as shown in Fig. 9). From the figure, it can be seen that the VTCs are intersecting at a single point, which is the indication of successful write operation.

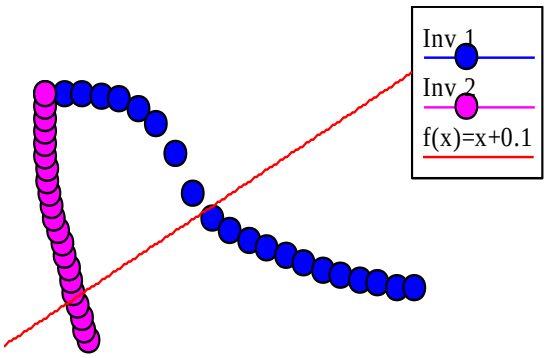

Figure 9. Butterfly Curve for Write Noise Margin of proposed 9T SRAM Cell.

The length of maximum diagonal inside the butterfly curve is found 0.4991.

So, SNM = Maximum length of diagonal of square / √ 2.

SNM = 0.4991/√ 2 = 0.352V at 1v power supply.

Write noise margin of proposed 9T SRAM Cell is as same as the Write noise margin of conventional 6T SRAM Cell because in write mode proposed circuit works like same as the conventional 6T SRAM Cell.

(c) Leakage power- Leakage power is the power dissipation of the SRAM Cell during standby mode. Figure shows the comparison of leakage power of different SRAM Cell .

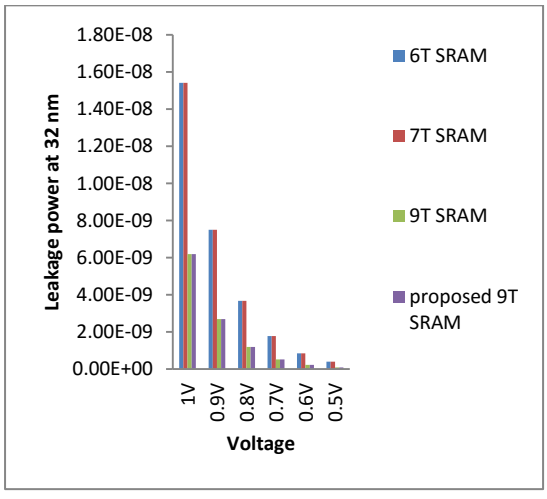

Figure 10. Leakage power comparison of different SRAM Cell.

It is clear from figure that the leakage power of proposed SRAM Cell is less as compared to other conventional SRAM Cells.

Table 2. Simulation Results for Different SRAM Cells

S. N.	Parameter	6T SRAM	7T SRAM	9T SRAM	Proposed 9T SRAM
1	Technology	32 nm	32nm	32nm	32nm
2	Supply voltage	1v	1v	1v	1v
3	Read delay	2.15 ps	2.21 ps	43.8 ps	44.7 ps
4	Read SNM	0.048 v	0.011 v	0.262v	0.262v
5	Leakage Power	15.4 nw	15.4 nw	6.18 nw	6.19 nw

As we can see from table 2 that the proposed cell has 79.06% shorter Read delay and 59.8% shorter leakage power as compare to conventional 6T SRAM Cell. Stability of proposed cell during Read mode is also improved. It offers 5.45x higher RSNM compare to conventional 6T SRAM Cell at 1v supply voltage at 32nm technology node.

4. Conclusion

This paper compared the performance parameters of four SRAM cell topologies, which include the conventional 6T, 7T, 9T and the proposed 9T SRAM cell implementations. In particular, the leakage power, Read delay and read behavior of each SRAM cells are being analyzed. The conventional 6T and 7T SRAM cells are the most area efficient have least transistor count. However, the leakage power becomes large and the read stability decreases due to undesirable time the basic latch consumes to read the cell during read operation, moreover the cell data is prone to corruption due to external noise. Even though 9T SRAM cell would simultaneously reduce leakage power and enhance data stability. To circumvent this problem the 9T SRAM cell design has been proposed in this research work, in which a transmission gate and NMOS Transistor are appended as a single-end read port. The results show that the proposed 9T SRAM always has less leakage power as compared to conventional 6T and 7T SRAM Cells, less Read delay and improve read stability as compared to the 6T, 7T, and 9T SRAM cells.

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