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RESEARCH ARTICLE

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A NOVEL BIST ARCHITECHTURE FOR AVODING SINGLE EVENT UPSETS IN FPGA

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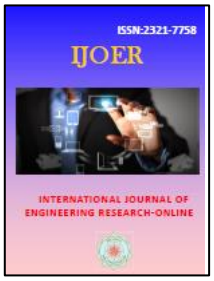


ABSTRACT
Field programmable gate arrays (FPGAs) pose a particularly difficult problem for test engineers due to their programmable nature, overall size and complexity, limited number of inputs/outputs (I/O), and large number and variety of embedded cores. In addition to manufacturing defects, "soft" errors due to single event upsets (SEUs) have become a serious problem because of the increasing size of the configuration memory in FPGAs and shrinking design rules, even in fault-tolerant systems operating at ground level. BIST configurations are presented for the configurable logic blocks (CLBs), I/O Tiles, and SEU detection/correction cores in Xilinx Virtex-5 FPGAs. This approach is particularly useful for in-system testing of FPGAs in fault-tolerant or high-reliability systems because it greatly reduces the amount and complexity of external hardware required for test. While not entirely immune to SEU effects, this approach greatly reduces the probability of an SEU induced failure in the user logic, and no single error from an SEU can cause a complete system failure.

Keywords— Built In Self-Test(BIST),Field Programmable Gate Array(FPGA),Single Event Upset(SEU),Configurable Logic Blocks(CLB),design for test(DFT).

1. INTRODUCTION

Radiation induced SEEs (Single Event Effects) in electronic systems are becoming a concern for reliability engineers. The origin of these effects is on ionized particles that hit the semiconductor releasing electron-hole pairs and provoking undesired currents. If these currents are able to provoke a voltage exceeding the threshold between logical '0' and logical '1' during a clock edge, an erroneous value is stored at a memory element. This effect is called SEU (Single Event Upset) and can provoke a functional failure if this error on the system state is propagated to the outputs. If the charged particle only flips one bit, the effect is called SBU (Single Bit Upset). MBU (Multi Bit Upset) happens when more than one memory cell results modified. The continuous transistor size reduction due to Moore's law is bringing lower supply voltages, reducing the threshold value between '0' and '1', increasing the probability of an SEU. Higher operating frequencies also increase the likelihood of these events to coincide with clock edges, increasing the failure rate[4].The exponential growth in the number of transistors on very large scale integration (VLSI) integrated circuits (ICs), coupled with increasing device interface bandwidth and new surface mount and low profile packaging technologies, have made testing of ICs increasingly difficult and costly at all levels of the testing process. The exponential growth in the number of transistors on very large scale integration (VLSI) integrated circuits (ICs), coupled with increasing device interface bandwidth and new surface mount and low profile packaging technologies, have made testing of ICs increasingly difficult and costly at all levels of the testing process.

1.1 Built-In Self-Test (BIST)

As the complexity and size of ICs grew, test equipment became more sophisticated increasing the manufacturing cost to as much as 30 to 40 percent of the cost of production [2]. Because of the limitations of the conventional testing techniques, a new DFT technique called Built-In Self-Test (BIST) was developed.

BIST is a DFT technique in which testing is accomplished through built-in hardware features. The basic idea is to have a VLSI chip that tests itself. The typical BIST architecture is composed of three hardware modules in addition to the circuit under test (CUT), as shown in Figure 1.1. The Test Pattern Generator (TPG) generates the test patterns for the CUT. The Output Response Analyser (ORA) compares or analyses the test responses to determine correctness of the CUT[2]. The BIST controller is the central unit to control all the BIST operations including initialization and length of the BIST sequence. In a BIST system hierarchy, there are BIST controllers at each level of the circuit hierarchy, such as module, chip, board, and system levels. Each BIST controller is responsible for the self-test in that particular level, the control of BIST operations for the lower level BIST, and the reporting of the test results to the upper level . The design of a TPG is determined by the test strategy being deployed. The test strategy being selected is determined by the fault coverage, test hardware overhead, and testing time[5][6].

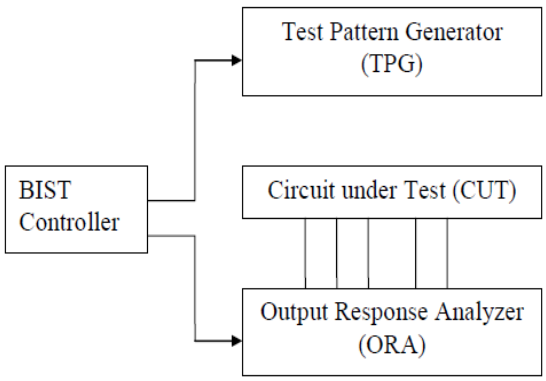


Figure-1.1: BIST architecture.

2.Built-In Self-Test for Virtex-4 and Virtex-5

A Built-In Self-Test (BIST) approach is presented for the Internal Configuration Access Port (ICAP) and Frame Error Correcting Code (ECC) logic cores embedded in Xilinx Virtex-4 and Virtex-5 Field Programmable Gate Arrays (FPGAs)[8]. The Frame ECC logic facilitates the detection of Single Event Upsets (SEUs) in the FPGA configuration memory. The ICAP provides read and write access to the configuration memory from within the FPGA fabric, enabling embedded dynamic reconfiguration and fault-tolerant applications with memory scrubbing. Therefore, the fault-free operation of the ICAP and Frame ECC logic is critical for space and fault-tolerant applications that require detection and repair of SEUs. The BIST approach presented is applicable to all Virtex-4 and Virtex-5 FPGAs for both manufacturing and system-level testing of the ICAP and Frame ECC logic. The actual implementation of the BIST approach in Virtex-4 and Virtex-5 FPGAs and associated experimental results are discussed.The increased use of Field Programmable Gate Arrays (FPGAs) for implementing digital logic applications over the past two decades has been accompanied by increased concern about radiation effects; in particular, the effects of Single Event Upsets (SEUs)[4]. In addition to memory elements, such as flip-flops and random access memories (RAMs), the contents of the static random access memory (SRAM) used as the configuration memory to establish the overall application performed by the FPGA is also susceptible to SEUs[9]. An SEU induced bit-flip in the SRAM configuration memory can alter the functionality of the FPGA. This makes SEUs of significantly more concern in FPGAs than in traditional application specific integrated circuits (ASICs). Radiation experiments indicate the SEU rate in FPGAs increased by a factor of 4.74 when design rules decreased from 600nm to 350nm with a corresponding reduction in Vcc supply voltage from 5V to 3.3V [7][8].

2.1 Frame ECC and ICAP Logic

Virtex-4 and Virtex-5 FPGAs provide a specialized core, called Frame ECC, for detection and identification of single-bit errors and detection of double-bit errors in the frame data [7]. Each time that a frame is read from the configuration memory the Frame ECC module calculates the Hamming bits as well as overall parity for the frame data, and compares these bits with the Hamming bits and parity stored for that frame in the configuration memory. Based on this comparison, the Frame ECC

module produces indications for no error, single-bit error, and double-bit error in addition to a syndrome indicating the location of single-bit errors. The error codes for the Frame ECC are summarized in Table 2.1.

Table-2.1: Frame ECC Codes.

Error Type	Condition (when *syndromevalid* = 1)
No bit error	Hamming match w/ no parity error
1-bit correctable error (SEC)	Hamming mismatch w/ parity error
2-bit error detection (DED)	Hamming mismatch w/ no parity error

A Hamming mismatch with an overall parity error indicates that a single-bit correctable error has occurred. In this case, the bit-wise exclusive-OR of the stored Hamming code and the regenerated Hamming code, which is called the *syndrome*, gives the location of the single-bit error. A Hamming mismatch (non-zero syndrome) and no overall parity error indicate a non correctable double-bit error has occurred. In the case of a double-bit error, the frame data must be repaired with data from a reliable external source. Single-bit errors in the configuration memory can be repaired with additional user logic implemented in the FPGA fabric to flip the bit in error as was done in[10] [11][13]. The SYNDROMEVALID output is asserted for one clock cycle per frame during a frame read operation to indicate that the SYNDROME and ERROR outputs are valid for the current frame. The most significant bit of the SYNDROME bus is the overall parity error indication. The ERROR output is asserted when a single-bit or double-bit error is detected[1][3]. To distinguish between single-bit correctable errors and double-bit non-correctable errors, the user must add logic to determine the result based on the scenarios in the last two entries in Table 2.1.

3. CONCLUSION

BIST approach for the ICAP and Frame ECC modules in Virtex-4 and Virtex-5 FPGAs. These modules are critical components used for SEU detection and correction in the configuration memory of FPGAs for space and fault-tolerant applications. The BIST approach was developed in VHDL and is applicable to all Virtex-4 and Virtex-5 devices, and the only overhead is the memory required to store the BIST configuration. The total test time is independent of the size of the FPGA.

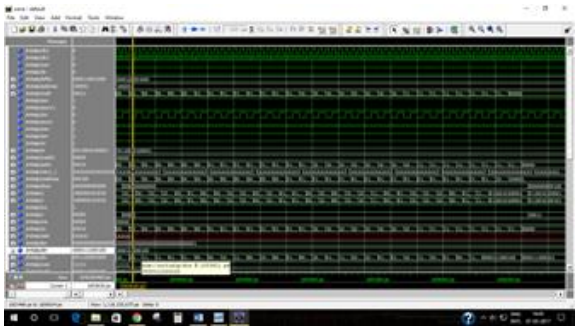
RESULTS

RTL Schematic

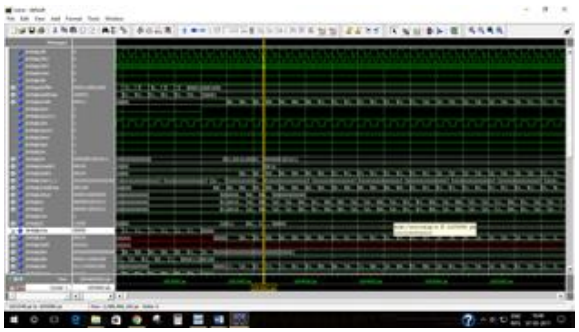
Initially write test patterns into the memory, for those test patterns we do error calculation and in below screenshot signals c ,ra(read address) used to identify the error position in memory ,based on signal c value we flip the error bit and store it into corresponding memory location.

If **c** value is “0000” then it indicates that there is no error, if c value other than “0000” then there is an error In corresponding memory location indicated signal ra.

This screen shot is showing that there is no error in memory location “00010” indicated by signal ra. because for this location value of signal c is “00000”.



Below screenshot is showing that there is error in memory location “00010” indicated by signal ra,because for this location value of signal c is “11000”.Signal c(3 down to 0) indicates that 8th bit of location “00010” is having error.



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