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RESEARCH ARTICLE

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DESIGN OF A LOW POWER FLIP-FLOP USING CMOS DEEP SUBMICRON TECHNOLOGY

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ABSTRACT

In this paper a novel technique is proposed based on the low power design of flip flop using Low power Clocked Pass Transistor Flip-Flop (LCPTFF) approach. The technique used in this paper is sleep transistor method for reduction of power consumption which is showing better result than the previously said technique. This method will reduce the power consumption by using sleep transistors which are used as switches and on or off condition, hence make the transistors go in sleep condition in when they are not in usage condition. This method is used in the deep submicron technology and hence the technique is named as Design of A Low Power Flip-Flop Using CMOS deep submicron technology. The simulations are done using Micro wind and DSCH analysis software tools and the results are shown for 5 transistor, 6 transistor and 8 transistor latch up circuits.

Keywords: Flip-flop, Deep Submicron Technology, Sleep Transistors, DSCH, Micro wind.

INTRODUCTION

The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially.

Today leakage power has become an increasingly important issue in processor hardware and software design. In 65 nm and below technologies, leakage accounts for 30-40% of processor power. In this paper, we propose a new sleep transistor approach which is CMOS deep submicron technology for reducing both leakage and dynamic powers. Moreover, the novel sleep transistor approach shows the least speed power product when compared to the existing methods.

VLSI is the process of creating integrated circuits by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being

developed. The microprocessor is a VLSI device. The first semiconductor chips held two transistors each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device.

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit; Static power: Includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling. Among these, sub threshold leakage is the most prominent one. Dynamic power: Includes charging and discharging power and short circuit power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower.

So it is becoming more and more important to reduce leakage power as well as dynamic power. There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limits its application. In this paper, we propose a novel dual stack technique that reduces not only leakage power but also dynamic power. We summarized and compared the previous techniques with our new approach.

Lowering supply voltage is effective for power reduction because of the quadratic relationship between supply voltage and dynamic power consumption. To compensate the performance loss due to a lower supply voltage, transistor threshold voltage has to be decreased as well, which causes exponential increase in the sub threshold leakage current. To reduce leakage power, multi threshold CMOS has been proposed with low blocks connected to ground through high transistors named as sleep transistors. The sleep transistor is turned on when the circuit is in the computational mode, and is turned off to cutoff the power supply in the standby mode for significant power reduction.

In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this technology trend, transistor leakage power has increased exponentially .As the feature size becomes smaller, shorter channel lengths result in increased sub threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub threshold leakage current because transistors cannot be turned off completely.

For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique.

We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this paper.

Leakage power has been increasing exponentially with the technology scaling. In 90nm node, leakage power can be as much as 35% of chip power. Consequently, leakage power reduction becomes critical in low-power applications such as cell phone and handheld terminals. Power-gating is the most effective standby leakage reduction method recently developed. In the power gating, sleep transistors are used as switches to shut off power supplies to parts of a design in standby mode. Although the concept of the sleep transistor is simple, design of a correct and optimal sleep transistor is challenge because of many effects introduced by the sleep transistor on design performance, area, rout ability, overall power dissipation, and signal/power integrity. Currently, many of the effects have not been fully aware by designers.

This could result in improper sleeper transistor design that would either fail to meet power reduction target when silicon is back or cause chip malfunction due to serious power integrity problems introduced. We have carried out comprehensive investigations on various effects of sleep transistor design and

implementations on chip performance, power, area and reliability. In this paper, we shall describe a number of critical considerations in the sleep transistor design and implementation including header or footer switch selection, sleep transistor distribution choices and sleep transistor gate length, width and body bias optimization for area, leakage and efficiency.

CMOS DEEP SUBMICRON TECHNOLOGY USING SLEEP TRANSISTOR METHOD

A sleep transistor is referred to either a PMOS or NMOS high Vth transistor that connects permanent power supply to circuit power supply which is commonly called “virtual power supply”. The sleep transistor is controlled by a power management unit to switch on and off power supply to the circuit.

The most well-known traditional approach is the sleep approach. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. Fig3.7 shows its structure. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively.

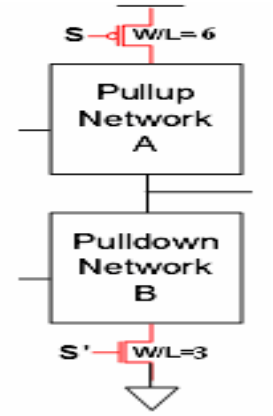

Figure 1: Sleep Transistor Method Design

LOW POWERCLOCKEDPASSTRANSISTOR FLIP-FLOP DESIGN

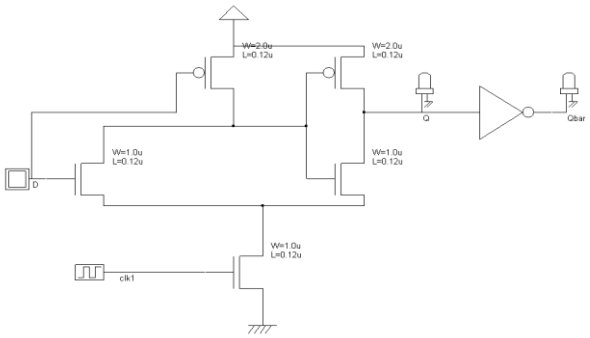

Figure 2:Low Power clocked Pass Transistor Flip-Flop Design

By using the Pass Transistor Logic family idea we are designing this circuit as well as by using the pass transistor logic we are using only one clocking transistor so it will be consuming only less power in the clock network of the Flip flop when compared to all other circuits. As well as we are having only 6 Transistors excluding the not gates also. So we will be having much reduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption. So this circuit will be acting as good sequential elements when compared to other flip-flop design

OUR PROPOSED SLEEP TRANSISTOR METHOD DESIGN:

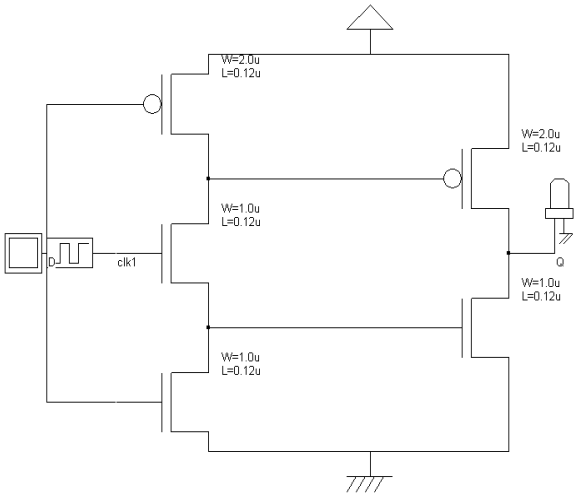

Figure 3:Sleep Transistor Method Flip-Flop Design

This figure shows positive edge triggered 5 Transistor D latch. When CLK and input IN are high then the transistors M1, M5 are OFF and remaining transistors M2, M3, M4 are ON. The output becomes high. During ON clock period whatever is the value of input it becomes output. It also acts as a flip-flop when the input IN has less pulse width. Minimization power consumption is essential for high performance VLSI systems. In digital CMOS circuits there are three sources of power dissipation, the first is due to signal transition, the second comes from short circuit current which flows directly from supply to ground terminal and the last is due to leakage currents. As technology scales down the short circuit power becomes comparable to dynamic power dissipation. Furthermore, the leakage power also becomes highly significant. High leakage current is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power especially for low-power applications.

DSCH is software for logic design. Based on primitives, a hierarchical circuit can be built and simulated. It also includes delay and power consumption evaluation. Silicon is for 3D display of the atomic structure of silicon, with emphasis on the silicon lattice, the do pants, and the silicon dioxide.

The Micro wind program allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. Microwind includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, Verilog compiler, tutorial on MOS devices).

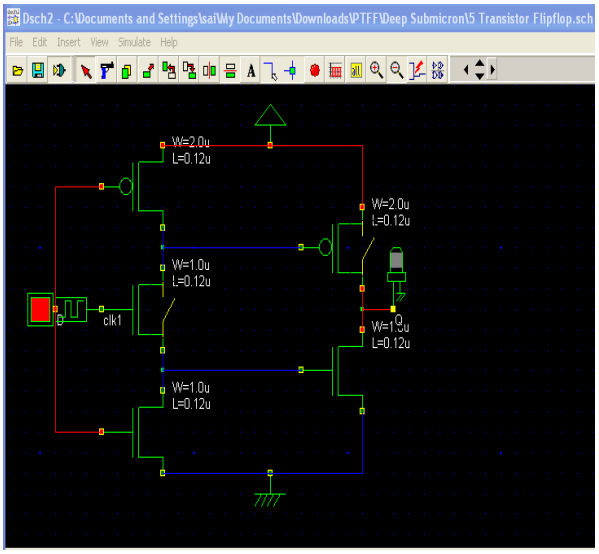

Figure 4: 5 Transistor Latchup circuit without Sleep Transistors

This figure shows the 5 transistor latchup circuit without sleep transistors in the DSCH tool.

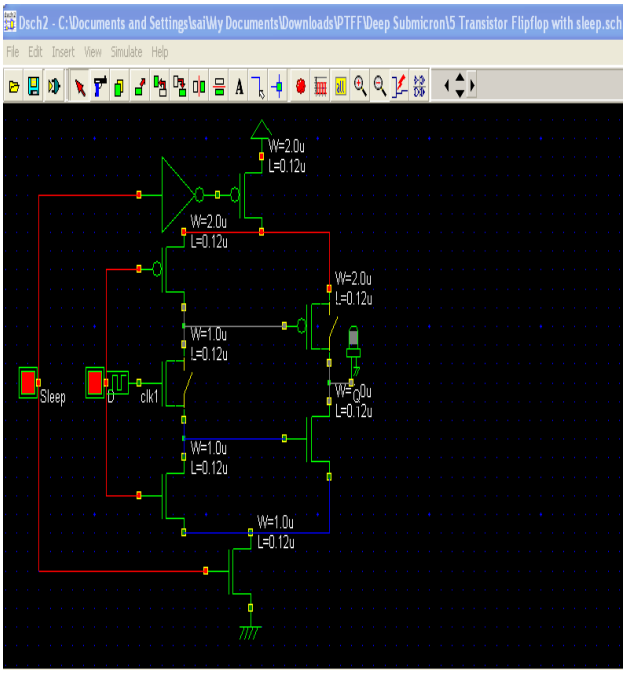

Figure5:5 Transistor latchup circuit with Sleep Transistors

This figure shows the 5 transistor latchup circuit with sleep transistors in the DSCH tool.

LAYOUT AND SIMULATION OF THE DESIGNED SYSTEM

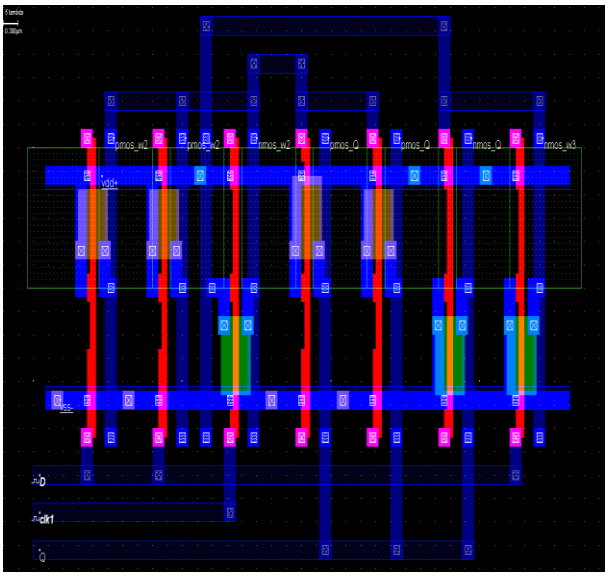

Figure 6: Layout Diagram of 5 Transistor latchup circuit without sleep transistors

This is the layout diagram of 5 transistor latchup circuit without sleep transistors in the Microwind.

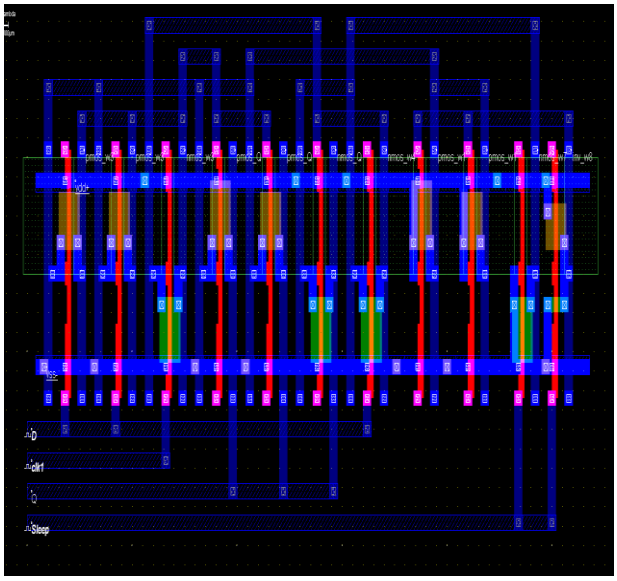

Figure 7: Layout Diagram of 5 Trnasistor latchup circuit with sleep transistors

This is the layout diagram of 5 transistor latchup circuit with sleep transistors in the Microwind.

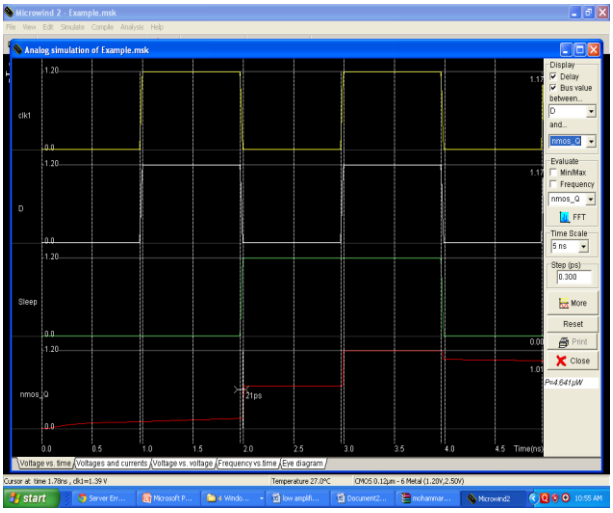

Figure 8: Simulation output of 5 Trnasistor latchup circuit without sleep transistors

This is the simulation output of 5 transistor latchup circuit without sleep transistors. The power consumption according to this circuit is totally 4.6041 micro watts.

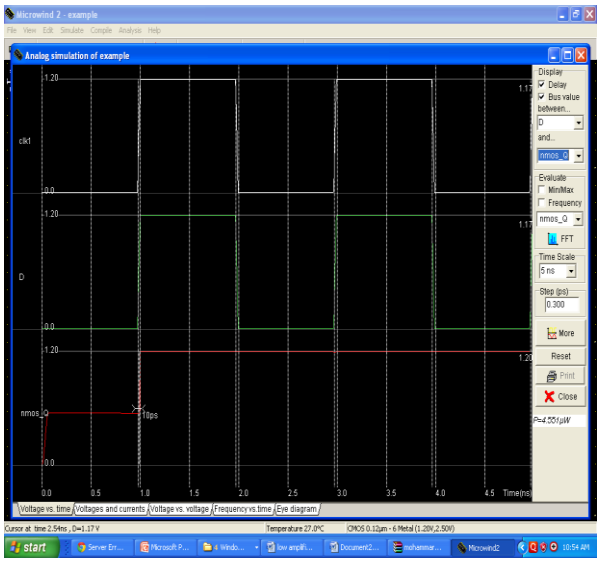

Figure 8: Simulation output of 5 Trnasistor latchup circuit without sleep transistors

This is the simulation output of 5 transistor latchup circuit with sleep transistors. The power consumption according to this circuit is totally 4.551 micro watts.

TABULATION OF POWER CONSUMPTION

Low Power clocked Pass Transistor Method- 9.581 micro watts

5 transistor latchup circuit without sleep-4.614 micro watts

5 transistor latchup circuit with sleep-4.551 micro watts

6 transistor latchup circuit without sleep-0.359 milli watts

6 transistor latchup circuit with sleep-0.212 mlli watts

8 transistor latchup circuit without sleep-25.504 micro watts

8 transistor latchup circuit with sleep-24.745 micro watts

CONCLUSION

In this Paper we proposed a new flip flop design using CMOS Deep Submicron Technology using sleep transistor method. The Proposed system shows Power improvement than the Low Power clocked Pass Transistor flip-flop which will lead to improvement in the case implementation in future mobile devices. In future it can be very suitable for System On Chip SOC applications which will lead us to a brighter tomorrow with low power consumption. This can be much suitable for application of battery oriented operation for less power and area. In future we can add some other leakage reduction techniques and the power can be further reduced.

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